PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-295697
(43)Date of publication of application : 29.10.1999

(51)Int.Cl. G02F 1/133
G09G 3/36
H04N 5/66

(21)Application number : 10-105226
(22)Date of filing : 15.04.1998

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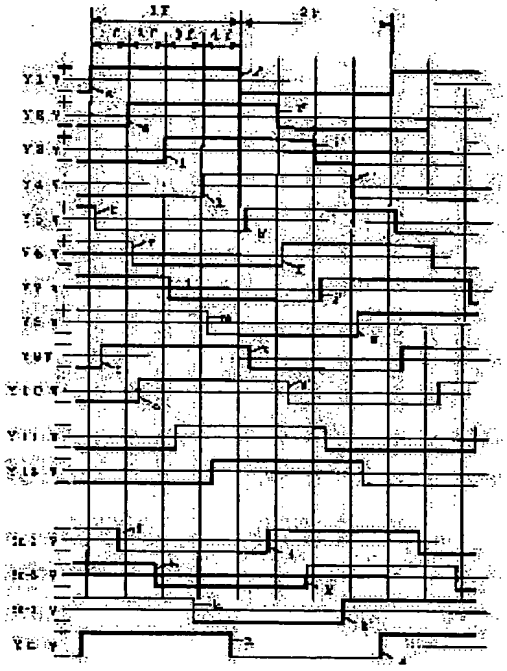
(54) DRIVING METHOD FOR LIQUID CRYSTAL DISPLAY DEVICE AND ELECTRONIC EQUIPMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To attain prevention of flickering in a picture or improvement in the non-uniformity of display by providing the term of inverting the polarity of a voltage to be applied to respective pixels on a scanning line in respect to the adjacent scanning line and the term of making the polarity equal within one frame period.
SOLUTION: In a first frame 1F, first of all, interlaced scanning is performed in a first field 1f for each of gate lines Y1, Y5, Y9...Yn-3 and each of four lines, selection is performed and writing is executed. On the gate lines Y1 and Y9, writing is performed with the positive polarity and on the gate lines Y5...Yn-3, writing is performed with the negative polarity. Thus, the polarity of a writing voltage is successively selected while being inverted by interlaced scanning for each of four lines. Concerning the voltage to be applied to the respective pixels on the respective gate lines, the period of a polarity inverted from the voltage applied to the respective upper and lower adjacent pixels exists only at one part of the entire voltage applying period and in the remaining period, the polarity can be made equal. Thus, the generation of discrination line can be reduced and improvement in contrast and luminance is enabled.



LEGAL STATUS

[Date of request for examination] 13.03.2003
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

[Claim(s)]
[Claim 1] The polarity of the electrical potential difference impressed to each pixel on the 1st scanning line in the liquid crystal display of the active-matrix mold which prepared the switching element in each pixel is the actuation approach of the liquid crystal display characterized by to have the 2nd period used as the 1st period which serves as reversed polarity on the basis of the potential of a common electrode, and like-pole nature to the polarity of the electrical potential difference impressed to each pixel on said 1st scanning line and the adjoining scanning line in an one frame period.
[Claim 2] The actuation approach of the liquid crystal display according to claim 1 characterized by comparing the electrical potential difference impressed to each pixel on the 1st scanning line with the electrical potential difference impressed to each pixel on the scanning line of the both sides of the 1st scanning line, and the sum total of said 1st period becoming almost the same to every scanning line.
[Claim 3] It is the actuation approach of the liquid crystal display according to claim 1 to 2 which divides an one-frame period into the sub period of N (N is two or more integers) individual, and is characterized by each sub period reversing the polarity of applied voltage for every scan period with a jump for every N scanning line.
[Claim 4] It is the actuation approach of the liquid crystal display according to claim 3 which divides an one-frame period into the sub period of N (integer of 2<=N<=32) individual, and is characterized by each sub period reversing the polarity of applied voltage for every scan period with a jump for every N scanning line.
[Claim 5] The actuation approach of the liquid crystal display according to claim 3 characterized by replacing the sequence of the scanning line scanned for said every sub selection period.
[Claim 6] The actuation approach of a liquid crystal display given in five from claim 1 characterized by the polarity of the electrical potential difference impressed to each pixel on the same scanning line being the same.
[Claim 7] The polarity of the electrical potential difference impressed to each pixel on the same scanning line is the actuation approach of a liquid crystal display given in five from claim 1 characterized by being reversed polarity on the basis of the potential of a common electrode every [every pixel and] 2 pixels.
[Claim 8] Electronic equipment characterized by having a liquid crystal display using the actuation approach given in seven from claim 1.

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the actuation approach of the liquid crystal display of an active matrix especially about the actuation approach of a liquid crystal display. Moreover, it is related with electronic equipment equipped with the liquid crystal display using the actuation approach of the liquid crystal display of an active matrix, and its liquid crystal display.
[0002]
[Description of the Prior Art] There is the actuation approach which is indicated by JP,5-29916,B as the actuation approach of the liquid crystal display of the conventional active matrix.
[0003] This actuation approach is the actuation approaches, like the approach of making reverse the polarity of the electrical potential difference impressed to each pixel for every scanning line as (a) of drawing 9 shows, and the polarity of the electrical potential difference impressed to each pixel as (b) shows make it reverse into next doors. This actuation approach sets prevention of CHIRATSUKI of a screen, the improvement of display nonuniformity, etc. as the main objects.
[0004]
[Problem(s) to be Solved by the Invention] In the case of such an actuation approach, when the polarity of the electrical potential difference impressed to the pixel of next doors is reverse as shown in drawing 8 R> 8 since the electrical potential difference impressed to the pixel of next doors becomes reversed polarity in almost all the periods of an one-frame period, a disclination line will occur.
[0005] for example, the configuration of the high-reflective-liquid-crystal light valve shown in drawing 7 -- 71 -- a polarization means and 72 -- the orientation film and 77 by the silicon substrate [a glass substrate and 73] [a transparent electrode and 74] [the orientation film and 75] [liquid crystal and 76] A circuit as shown on this silicon substrate 77 at drawing 6 is constituted, and a dielectric constant anisotropy puts a negative nematic liquid crystal into a dip vertical orientation cel, and liquid crystal 75 makes an example the case in the liquid crystal mode which becomes dark in the condition of not impressing

an electrical potential difference to liquid crystal, and explains it.

[0006] Impressing and white-displaying ON state voltage on each pixel, the disclination line generated when the polarity of the electrical potential difference impressed to the pixel of next doors is reverse becomes dark. The situation of this disclination line generating is shown in drawing 8 . 81-84 express each pixel and + and - express the polarity of the electrical potential difference currently impressed to each pixel. And 85-88 express the situation of generating of the disclination line generated in each pixel. Thus, a dark disclination line will occur near the borderline of each pixel. This disclination line will cause image quality lowering, such as lowering of contrast, and lowering of brightness.

[0007] And if highly minute-ization progresses like recently and the size which is 1 pixel becomes small, the rate of the generating area of a disclination line to pixel area will increase, and deterioration of image quality will become more serious.

[0008] Especially the light valve used for a liquid crystal projector etc. has a small screen size, and since highly minute-ization is demanded, it tends to be influenced too many. Also in it, in the case of the liquid crystal light valve of a reflective mold as shown in JP,9-236814,A, the clearance between each pixel is small, moreover, since pixel size is also small, the effect of a disclination line will be large and image quality will also deteriorate.

[0009] Moreover, although the polarity of the electrical potential difference impressed to all pixels can be made the same and only polar reversal for every frame can also be carried out in order not to generate a disclination line, CHIRATSUKI will occur.

[0010]

[Means for Solving the Problem] The polarity of the electrical potential difference which impresses a liquid crystal display according to claim 1 to each pixel on the 1st scanning line in the liquid crystal display of the active-matrix mold which prepared the switching element in each pixel It is characterized by having the 2nd period used as the 1st period which serves as reversed polarity on the basis of the potential of a common electrode, and like-pole nature to the polarity of the electrical potential difference impressed to each pixel on said 1st scanning line and the adjoining scanning line in an one-frame period.

[0011] According to the above-mentioned configuration, generating of the disclination line generated when the polarity of the electrical potential difference impressed to the adjoining pixel is reverse can be reduced, and it has the effectiveness that the brightness and contrast of a liquid crystal display can be improved.

[0012] A liquid crystal display according to claim 2 compares the electrical potential difference impressed to each pixel on the 1st scanning line with the electrical potential difference impressed to each pixel on the scanning line of the both sides of the 1st scanning line, and is characterized by the sum total of said 1st period becoming almost the same to every scanning line.

[0013] According to the above-mentioned configuration, generating of the disclination line generated when the polarity of the electrical potential difference impressed to the adjoining pixel is reverse can be reduced, and it has the effectiveness that the brightness and contrast of a liquid crystal display can be improved.

[0014] A liquid crystal display according to claim 3 divides an one-frame period into the sub period of N (N is two or more integers) individual, and each sub period is characterized by reversing the polarity of applied voltage for every scan period with a jump for every N scanning line.

[0015] According to the above-mentioned configuration, generating of the disclination line generated when the polarity of the electrical potential difference impressed to the adjoining pixel is reverse can be reduced, and it has the effectiveness that the brightness and contrast of a liquid crystal display can be improved.

[0016] A liquid crystal display according to claim 4 divides an one-frame period into the sub period of N (integer of 2<=N<=32) individual, and each sub period is characterized by reversing the polarity of applied voltage for every scan period with a jump for every N scanning line.

[0017] According to the above-mentioned configuration, generating of the disclination line generated when the polarity of the electrical potential difference impressed to the adjoining pixel is reverse can be reduced, and it has the effectiveness that it can improve and optimization of a control circuit can also do the brightness and contrast of a liquid crystal display.

[0018] A liquid crystal display according to claim 5 is characterized by replacing the sequence of the scanning line scanned for said every sub selection period.

[0019] According to the above-mentioned configuration, generating of the disclination line generated when the polarity of the electrical potential difference impressed to the adjoining pixel is reverse can be reduced, and it has the effectiveness that it can improve and reduction of CHIRATSUKI can also do the brightness and contrast of a liquid crystal display.

[0020] A liquid crystal display according to claim 6 is characterized by the polarity of the electrical potential difference impressed to each pixel on the

same scanning line being the same.

[0021] According to the above-mentioned configuration, generating of the disclination line generated when the polarity of the electrical potential difference impressed to the adjoining pixel is reverse can be reduced, and it has the effectiveness that the brightness and contrast of a liquid crystal display can be improved.

[0022] The polarity of the electrical potential difference which impresses a liquid crystal display according to claim 7 to each pixel on the same scanning line is characterized by being reversed polarity on the basis of the potential of a common electrode every [every pixel and] 2 pixels.

[0023] According to the above-mentioned configuration, generating of the disclination line generated when the polarity of the electrical potential difference impressed to the adjoining pixel is reverse can be reduced, and it has the effectiveness that it can improve and reduction of CHIRATSUKI can also do the brightness and contrast of a liquid crystal display.

[0024] Electronic equipment according to claim 8 is characterized by having the liquid crystal display which used the actuation approach given in seven from claim 1.

[0025] According to the above-mentioned configuration, it has the effectiveness that it is bright, contrast is high, it is legible, and the high electronic equipment of display quality can be offered.

[0026]

[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained based on a drawing.

[0027] In addition, this examples 1-6 are the active matrices which prepared the transistor in each pixel, as shown in drawing 6 , and they raise and explain to an example the high-reflective-liquid-crystal light valve shown in drawing 7 .

[0028] drawing in which 601 of drawing 6 (a) shows an example of the equal circuit of the pixel section -- it is -- 602 -- a transistor -- it is -- 603 -- liquid crystal and 607 show retention volume and 608 shows [the gate of a transistor, and 604 / the source of a transistor, and 605 / the drain of a transistor and a pixel electrode, and 606] the common electrode, respectively. and (b) -- with the block diagram of an example of the actuation circuit of an active matrix liquid crystal indicating equipment, a gate line driver, and Y1-Yn show a gate line, and X1-Xm show [611 / a signal-line driver and 612] the source line, respectively.

[0029] And as shown in drawing 6 (b), the gate 603 of each pixel shown by 601 was connected with the gate line, and the source 604 is connected with the source line.

[0030] Moreover, drawing 7 is drawing showing an example of the configuration of a high-reflective-liquid-crystal light valve, and the circuit as the orientation film and 77 are [a glass substrate and 73 / a transparent electrode and 74 / liquid crystal and 76] silicon substrates for the orientation film and 75 and a polarization means and 72 show on this silicon substrate 77 at drawing 6 is constituted for 71. And a dielectric constant anisotropy puts a negative nematic liquid crystal into a dip vertical orientation cel, and liquid crystal 75 makes an example the case in the liquid crystal mode which becomes dark in the condition of not impressing an electrical potential difference to liquid crystal, and explains it.

[0031] (Example 1) Drawing 1 shows the polarity of the timing by which an electrical potential difference is written in the pixel of each scanning-line direction of the display shown in drawing 5 (a), and an electrical potential difference. Driving by dividing into the 4 field the polarity of the electrical potential difference impressed to the pixel of the direction of the scanning line by the case of being the same, Y1-Yn of drawing 1 show the condition that continue after writing is performed at the timing and one selection period which are turning on and writing in the transistor of each pixel on each gate line of Y1-Yn of drawing 6 (b), and the electrical potential difference is held with the polarity as it is. The polarity of the electrical potential difference impressed to each pixel is expressed with forward and negative on the basis of the potential V of the common electrode 608 (the common electrode 608 shows the transparent electrode 73 of drawing 7 .) of drawing 6 .

[0032] In 1F of drawing 1 , 2F express the 2nd frame with the 1st frame.

[0033] the 1st field first shown by 1f with the 1st frame -- the gate lines Y1, Y5, and Y9 and ... Yn-3 and interlaced scanning in every four lines are performed, selection is made and writing is performed. As for Y1, Y9, and ... (gate line which corresponds every eight lines from Y1), writing is performed with straight polarity, and, as for Y5, ..., Yn-3 (gate line which corresponds every eight lines from Y5), writing is performed by negative polarity. It holds to the timing of a' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y1 between one selection periods to the timing of a, and is written in a degree. And in the next selection period, it holds to the timing of b' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y5 between one selection periods to the timing of b, and is written in a degree. And in the next selection

period, the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y9 between one selection periods to the timing of c, and it is written in a degree, and holds to timing ** of c' of the 2nd frame. Thus, sequential selection is made, and it goes by interlaced scanning in every four lines, reversing the polarity of a write-in electrical potential difference, and holds to the timing of d' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in gate line Yn-3 between one selection periods to the timing of d, and is written in a degree. The 2nd field which 1 field period (1f) ends now, and is shown by the following 2f is started.

[0034] the 2nd field -- the gate lines Y2, Y6, and Y10 and ... Yn-2 and interlaced scanning in every four lines are performed, selection is made and writing is performed. As for Y2, Y10, and ... (gate line which corresponds every eight lines from Y2), writing is performed with straight polarity, and, as for Y6, ..., Yn-2 (gate line which corresponds every eight lines from Y6), writing is performed by negative polarity. It holds to the timing of e' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y2 between one selection periods to the timing of e, and is written in a degree. And in the next selection period, it holds to the timing of f' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y6 between one selection periods to the timing of f, and is written in a degree. And in the next selection period, it holds to the timing of g' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y10 between one selection periods to the timing of g, and is written in a degree. Thus, sequential selection is made, and it goes by interlaced scanning in every four lines, reversing the polarity of a write-in electrical potential difference, and holds to the timing of h' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in gate line Yn-2 between one selection periods to the timing of h, and is written in a degree. The 3rd field which 2 field period ends now and is shown by the following 3f starts.

[0035] In the 3rd field, the gate lines Y3, Y7, and Y11, ..., Yn-1, and interlaced scanning in every four lines are performed, selection is made and writing is performed. As for Y3, Y11, and ... (gate line which corresponds every eight lines from Y3), writing is performed with straight polarity, and, as for Y7, ..., Yn-1 (gate line which corresponds every eight lines from Y7), writing is performed by negative polarity. It holds to the timing of i' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y3 between one selection periods to the timing of i, and is written in a degree. And in the next selection period, it holds to the timing of j' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y7 between one selection periods to the timing of j, and is written in a degree. And in the next selection period, it holds to the timing which was late for j' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y11 between one selection periods to the timing which was late for j during the 1 selection, and is written in a degree during the 1 selection. Thus, sequential selection is made, and it goes by interlaced scanning in every four lines, reversing the polarity of a write-in electrical potential difference, and holds to the timing of k' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in gate line Yn-1 between one selection periods to the timing of k, and is written in a degree. The 4th field which 3 field period ends now and is shown by the following 4f is started.

[0036] In the 4th field, the gate lines Y4, Y8, Y12, ..., Yn and interlaced scanning in every four lines are performed, selection is made and writing is performed. As for Y4, Y12, and ... (gate line which corresponds every eight lines from Y4), writing is performed with straight polarity, and, as for Y8, ..., Yn (gate line which corresponds every eight lines from Y8), writing is performed by negative polarity. It holds to the timing of l' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y4 between one selection periods to the timing of l, and is written in a degree. And in the next selection period, it holds to the timing of m' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y8 between one selection periods to the timing of m, and is written in a degree. And in the next selection period, it holds to the timing which was late for m' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y12 between one selection periods to the timing which was late for m during the 1 selection, and is written in a degree during the 1 selection. Thus, sequential selection is made, and it goes by interlaced scanning in every four lines, reversing the polarity of a write-in electrical potential difference, and holds to the timing of n' of the 2nd frame which the electrical potential difference by

the side of negative polarity is written in the gate line Yn between one selection periods to the timing of n, and is written in a degree. 4 field period expires now, the 1st frame is completed, and then the 2nd frame is started.

[0037] He is trying for the 2nd frame to write an electrical potential difference in each pixel with the 1st frame and reversed polarity in the same way as the 1st frame. And this actuation is repeated and alternating current actuation of each pixel is carried out.

[0038] The electrical potential difference impressed to the source line shown by X1-Xm by carrying out such actuation, changing a polarity for every selection period For example, the applied voltage of each pixel on the gate line Y2 of drawing 6 (b) is received. If the electrical potential difference currently impressed to each pixel on the gate line Y1 on it is seen about the 1st frame period of drawing 1 , the period (2f-4f) of the remainder [period / (1f) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature. And if the electrical potential difference currently impressed to each pixel on the gate line Y3 under it is seen about the 1st frame period of drawing 1 to the applied voltage of each pixel on the gate line Y2, the period (1f and 3f-4f) of the remainder [period / (2f) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature.

[0039] Moreover, if the electrical potential difference currently impressed to each pixel on the gate line Y6 on it is seen about the 1st frame period of drawing 1 to the applied voltage of each pixel on the gate line Y7 of drawing 6 (b) The period of the remainder [period / (from the timing of f up to the timing of j) / in an one frame period / about 1 field] in reversed polarity becomes like-pole nature (from the timing of 1f to f, and the timing of j to 4f termination). And if the electrical potential difference currently impressed to each pixel on the gate line Y8 under it is seen about the 1st frame period of drawing 1 , the period of the remainder [period / (from the timing of j up to the timing of m) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature (from the timing of 1f to j, and the timing of m to 4f termination). Therefore, the sum total of the period used as the reversed polarity in the scanning line of the both sides which adjoin to every scanning line becomes almost equal to 2 field period (every [in vertical both sides / an one field each period]). (However, in the 1f of the 1 field periods of a frame period first [each], about the gate line by which a polarity is chosen by changing by interlaced scanning) The period to timing when writing is performed from initiation of 1f of 1 field periods to a gate line just before [that] adjoining, or the period when only the part of the difference of the period to timing when writing is performed from initiation of 1f of 1 field periods, and the period to timing when writing is performed from initiation of 1f of 1 field periods in front of 1 selection period serves as reversed polarity becomes large slightly.

Thus, since the period of the remainder [period / in the electrical potential difference which impresses the electrical potential difference impressed to each pixel on each gate line to each pixel of the adjacent upper and lower sides, and an one frame period / about 1 field] in reversed polarity can be made into like-pole nature, generating of a disclination line can be reduced, improvement in contrast and improvement in brightness can be attained, and it can improve image quality substantially.

[0040] In addition, as shown in drawing 5 (a), it explained by the approach of impressing an electrical potential difference to each pixel, but even if it reverses a polarity for every source line, or the above-mentioned example reverses a polarity for every two source lines as shown in drawing 5 (c) as shown in drawing 5 (b), it can be driven by the same approach.

[0041] Moreover, drawing shown by drawing 1 expresses the polarity of the electrical potential difference impressed to each pixel, and does not express the voltage level impressed actually. According to an indicative data, as for the electrical potential difference actually impressed to each pixel, a different electrical potential difference of a voltage level is impressed.

[0042] (Example 2) This example is the same actuation approach as an example 1, and is the actuation approach at the time of changing the number of the field periods divided at an one-frame period, and making it 8 field period.

[0043] Drawing 2 shows the polarity of the timing by which an electrical potential difference is written in the pixel of each scanning-line direction of the display shown in drawing 5 (a), and an electrical potential difference. Driving by dividing into the 8 field the polarity of the electrical potential difference impressed to the pixel of the direction of the scanning line by the case of being the same, Y1-Yn of drawing 2 show the condition that continue after writing is performed at the timing and one selection period which are turning on and writing in the transistor of each pixel on each gate line of Y1-Yn of drawing 6 (b), and the electrical potential difference is held with the polarity as it is. The polarity of the electrical potential difference impressed to each pixel is expressed with forward and negative on the basis of the potential V of the common electrode 608 (the common electrode 608 shows the transparent

electrode 73 of drawing 7 .) of drawing 6 .

[0044] In 1F of drawing 2 , 2F express the 2nd frame with the 1st frame.

[0045] With the 1st frame, first, the gate lines Y1 and Y9, ..., Yn-7, and interlaced scanning in every eight lines are performed, selection is made and writing is performed in the 1st field shown by 1f. Writing is performed with straight polarity and, as for Y1, Y17, ..., Yn-7 (gate line which corresponds every 16 lines from Y1), writing is performed by negative polarity, as for Y9, Y25, and ... (gate line which corresponds every 16 lines from Y9). It holds to the timing of a' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y1 between one selection periods to the timing of a, and is written in a degree. And in the next selection period, it holds to the timing of b' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y9 between one selection periods to the timing of b, and is written in a degree. Thus, it holds until make sequential selection, it goes by interlaced scanning in every eight lines, an electrical potential difference is written in to each pixel on gate line Yn-7 and it is written in a degree, reversing the polarity of a write-in electrical potential difference. The 2nd field which 1 field period ends now and is shown by the following 2f is started.

[0046] In the 2nd field, the gate lines Y2 and Y10, ..., Yn-6, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y2, Y18, ..., Yn-6 (gate line which corresponds every 16 lines from Y2), writing is performed by negative polarity, as for Y10, Y26, and ... (gate line which corresponds every 16 lines from Y10). It holds to the timing of c' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y2 between one selection periods to the timing of c, and is written in a degree. And in the next selection period, it holds to the timing of d' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y10 between one selection periods to the timing of d, and is written in a degree. Thus, it holds until make sequential selection, it goes by interlaced scanning in every eight lines, an electrical potential difference is written in to each pixel on gate line Yn-6 and it is written in a degree, reversing the polarity of a write-in electrical potential difference. The 3rd field which 2 field period ends now and is shown by the following 3f is started.

[0047] Thus, in the 3rd field, the gate lines Y3 and Y11, ..., Yn-5, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y3, Y19, ..., Yn-5 (gate line which corresponds every 16 lines from Y3), writing is performed by negative polarity, as for Y11, Y27, and ... (gate line which corresponds every 16 lines from Y11). It holds to the timing of e' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y3 between one selection periods to the timing of e, and is written in a degree. And a gate line is chosen by interlaced scanning in every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.

[0048] In the 4th field, the gate lines Y4 and Y12, ..., Yn-4, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y4, Y20, ..., Yn-4 (gate line which corresponds every 16 lines from Y4), writing is performed by negative polarity, as for Y12, Y28, and ... (gate line which corresponds every 16 lines from Y12). It holds to the timing of f' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y4 between one selection periods to the timing of f, and is written in a degree. And a gate line is chosen by interlaced scanning in every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.

[0049] In the 5th field, the gate lines Y5 and Y13, ..., Yn-3, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y5, Y21, ..., Yn-3 (gate line which corresponds every 16 lines from Y5), writing is performed by negative polarity, as for Y13, Y29, and ... (gate line which corresponds every 16 lines from Y13). It holds to the timing of g' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y5 between one selection periods to the timing of g, and is written in a degree. And a gate line is chosen by interlaced scanning in every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the

selected gate line and it is written in a degree.
[0050] In the 6th field, the gate lines Y6 and Y14, ..., Yn-2, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y6, Y22, ..., Yn-2 (gate line which corresponds every 16 lines from Y6), writing is performed by negative polarity, as for Y14, Y30, and ... (gate line which corresponds every 16 lines from Y14). It holds to the timing of h' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y6 between one selection periods to the timing of h, and is written in a degree. And a gate line is chosen by interlaced scanning in every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.
[0051] In the 7th field, the gate lines Y7 and Y15, ..., Yn-1, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y7, Y23, ..., Yn-1 (gate line which corresponds every 16 lines from Y7), writing is performed by negative polarity, as for Y15, Y31, and ... (gate line which corresponds every 16 lines from Y15). It holds to the timing of i' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y7 between one selection periods to the timing of i, and is written in a degree. And a gate line is chosen by interlaced scanning in every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.
[0052] In the 8th field, the gate lines Y8, Y16, ..., Yn and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y8, Y24, ..., Yn (gate line which corresponds every 16 lines from Y8), writing is performed by negative polarity, as for Y16, Y32, and ... (gate line which corresponds every 16 lines from Y16). It holds to the timing of j' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y8 between one selection periods to the timing of j, and is written in a degree. And a gate line is chosen by interlaced scanning in every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.
[0053] Thus, it ends to the 8th field, the 1st frame is completed, and then the 2nd frame is started.
[0054] He is trying for the 2nd frame to write an electrical potential difference in each pixel with the 1st frame and reversed polarity in the same way as the 1st frame. And this actuation is repeated and alternating current actuation of each pixel is carried out.
[0055] The electrical potential difference impressed to the source line shown by X1-Xm by carrying out such actuation, changing a polarity for every selection period For example, the applied voltage of each pixel on the gate line Y2 of drawing 6 (b) is received. If the electrical potential difference currently impressed to each pixel on the gate line Y1 on it is seen about the 1st frame period of drawing 2 , the period (2f-8f) of the remainder [period / (1f) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature. And if the electrical potential difference currently impressed to each pixel on the gate line Y3 under it is seen about the 1st frame period of drawing 2 to the applied voltage of each pixel on the gate line Y2, the period (1f and 3f-8f) of the remainder [period / (2f) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature.
[0056] Moreover, if the electrical potential difference currently impressed to each pixel on the gate line Y6 on it is seen about the 1st frame period of drawing 2 to the applied voltage of each pixel on the gate line Y7 of drawing 6 (b), the period (1f-5f, and 7f-8f) of the remainder [period / (6f) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature. And if the electrical potential difference currently impressed to each pixel on the gate line Y8 under it is seen about the 1st frame period of drawing 2 to the applied voltage of each pixel on the gate line Y7, the period (1f-6f, and 8f) of the remainder [period / (7f) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature. Therefore, the sum total of the period used as the reversed polarity in the scanning line of the both sides which adjoin to every scanning line becomes almost equal to 2 field period (every [in vertical both sides / an one field each period]). (However, in the 1f of the 1 field periods of a frame period first [each], about the gate line by which a polarity is chosen by changing by interlaced scanning) The period to timing when writing is performed from initiation of 1f of 1 field periods to a gate line just before [that] adjoining, or the period when only the part of the difference of the period to timing when writing is performed from

initiation of 1f of 1 field periods, and the period to timing when writing is performed from initiation of 1f of 1 field periods in front of 1 selection period serves as reversed polarity becomes large slightly. Thus, since the period of the remainder [period / in the electrical potential difference which impresses the electrical potential difference impressed to each pixel on each gate line to each pixel of the adjacent upper and lower sides, and an one frame period / about 1 field] in reversed polarity can be made into like-pole nature, generating of a disclination line can be reduced, improvement in contrast and improvement in brightness can be attained, and it can improve image quality substantially.

[0057] In addition, as shown in drawing 5 (a), it explained by the approach of impressing an electrical potential difference to each pixel, but even if it reverses a polarity for every source line, or the above-mentioned example reverses a polarity for every two source lines as shown in drawing 5 (c) as shown in drawing 5 (b), it can be driven by the same approach. (Although 4 pixels of polarities have reversed drawing 5 at a time in the direction of a gate line since it shows the case where divide an one-frame period into the 4 fields, and it is driven as shown in an example 1, this changes to every 8 pixels polarity reversals in the example 2.)

Moreover, drawing shown by drawing 2 expresses the polarity of the electrical potential difference impressed to each pixel like drawing 1 used by explanation of an example 1, and does not express the voltage level impressed actually. According to an indicative data, as for the electrical potential difference actually impressed to each pixel, a different electrical potential difference of a voltage level is impressed.

[0058] (Example 3) Drawing applied to an example 3 in drawing 3 is shown in drawing 3 .

[0059] Drawing shown by drawing 3 expresses the polarity of the electrical potential difference impressed to each pixel like drawing 1 used by explanation of examples 1 and 2, and 2, and does not express the voltage level impressed actually. According to an indicative data, as for the electrical potential difference actually impressed to each pixel, a different electrical potential difference of a voltage level is impressed. Moreover, the polarity of the electrical potential difference impressed to each pixel is expressed with forward and negative on the basis of the potential V of the common electrode 608 (the common electrode 608 shows the transparent electrode 73 of drawing 7 .) of drawing 6 .

[0060] In 1F of drawing 3 , 2F express the 2nd frame with the 1st frame.

[0061] the 1st field first shown by 1f with the 1st frame -- the gate lines Y1, Y5, and Y9 and ... Yn-3 and interlaced scanning in every four lines are performed, selection is made and writing is performed. As for Y1, Y9, and ... (gate line which corresponds every eight lines from Y1), writing is performed with straight polarity, and, as for Y5, ..., Yn-3 (gate line which corresponds every eight lines from Y5), writing is performed by negative polarity. It holds to the timing of a' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y1 between one selection periods to the timing of a, and is written in a degree. And in the next selection period, it holds to the timing of b' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y5 between one selection periods to the timing of b, and is written in a degree. And in the next selection period, it holds to the timing of c' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y9 between one selection periods to the timing of c, and is written in a degree. Thus, sequential selection is made, and it goes by interlaced scanning in every four lines, reversing the polarity of a write-in electrical potential difference, and holds to the timing of d' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in gate line Yn-3 between one selection periods to the timing of d, and is written in a degree. The 2nd field which 1 field period ends now and is shown by the following 2f is started.

[0062] In the 2nd field, the gate lines Y3, Y7, and Y11, ..., Yn-1, and interlaced scanning in every four lines are performed, selection is made and writing is performed. As for Y3, Y11, and ... (gate line which corresponds every eight lines from Y3), writing is performed with straight polarity, and, as for Y7, ..., Yn-1 (gate line which corresponds every eight lines from Y7), writing is performed by negative polarity. It holds to the timing of e' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y3 between one selection periods to the timing of e, and is written in a degree. And in the next selection period, it holds to the timing of f' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y7 between one selection periods to the timing of f, and is written in a degree. And in the next selection period, it holds to the timing which was late for f' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y11 between one selection periods to the timing which

was late for f during the 1 selection, and is written in a degree during the 1 selection. Thus, it holds to the timing of g' of the 2nd frame which writes in every four lines, and sequential selection is made, it goes, reversing the polarity of an electrical potential difference, and the electrical potential difference by the side of negative polarity is written in gate line Yn-1 between one selection periods to the timing of g, and is written in a degree. The 3rd field which 2 field period ends now and is shown by the following 3f is started.

[0063] the 3rd field -- the gate lines Y2, Y6, and Y10 and ... Yn-2 and interlaced scanning in every four lines are performed, selection is made and writing is performed. As for Y2, Y10, and ... (gate line which corresponds every eight lines from Y2), writing is performed with straight polarity, and, as for Y6, ..., Yn-2 (gate line which corresponds every eight lines from Y6), writing is performed by negative polarity. It holds to the timing of h' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y2 between one selection periods to the timing of h, and is written in a degree. And in the next selection period, it holds to the timing of i' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y6 between one selection periods to the timing of i, and is written in a degree. And in the next selection period, it holds to the timing of j' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y10 between one selection periods to the timing of j, and is written in a degree. Thus, sequential selection is made, and it goes by interlaced scanning in every four lines, reversing the polarity of a write-in electrical potential difference, and holds to the timing of k' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in gate line Yn-2 between one selection periods to the timing of k, and is written in a degree. The 4th field which 3 field period ends now and is shown by the following 4f is started.

[0064] In the 4th field, the gate lines Y4, Y8, Y12, ..., Yn and interlaced scanning in every four lines are performed, selection is made and writing is performed. As for Y4, Y12, and ... (gate line which corresponds every eight lines from Y4), writing is performed with straight polarity, and, as for Y8, ..., Yn (gate line which corresponds every eight lines from Y8), writing is performed by negative polarity. It holds to the timing of l' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y4 between one selection periods to the timing of l, and is written in a degree. And in the next selection period, it holds to the timing of m' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y8 between one selection periods to the timing of m, and is written in a degree. And in the next selection period, it holds to the timing which was late for m' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y12 between one selection periods to the timing which was late for m during the 1 selection, and is written in a degree during the 1 selection. Thus, sequential selection is made, and it goes by interlaced scanning in every four lines, reversing the polarity of a write-in electrical potential difference, and holds to the timing of n' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the gate line Yn between one selection periods to the timing of n, and is written in a degree. 4 field period expires now, the 1st frame is completed, and then the 2nd frame is started.

[0065] He is trying for the 2nd frame to write an electrical potential difference in each pixel with the 1st frame and reversed polarity in the same way as the 1st frame. And this actuation is repeated and alternating current actuation of each pixel is carried out.

[0066] The electrical potential difference impressed to the source line shown by X1-Xm by carrying out such actuation, changing a polarity for every selection period For example, the applied voltage of each pixel on the gate line Y2 of drawing 6 (b) is received. If the electrical potential difference currently impressed to each pixel on the gate line Y1 on it is seen about the 1st frame period of drawing 3 , the period (3f-4f) of the remainder [period / (1f-2f) / in an one frame period / about 2 field] in reversed polarity will become like-pole nature. And if the electrical potential difference currently impressed to each pixel on the gate line Y3 under it is seen about the 1st frame period of drawing 3 to the applied voltage of each pixel on the gate line Y2, the period (1f and 3f-4f) of the remainder [period / (2f) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature.

[0067] Moreover, if the electrical potential difference currently impressed to each pixel on the gate line Y6 on it is seen about the 1st frame period of drawing 3 to the applied voltage of each pixel on the gate line Y7 of drawing 6 (b) The period of the remainder [period / (from the timing of f up to the timing of i) / in an one frame period / about 1 field] in reversed polarity becomes like-pole nature (from the timing of 1 f-i, and the timing of i to 4f termination). And if the electrical

potential difference currently impressed to each pixel on the gate line Y8 under it is seen about the 1st frame period of drawing 3 , the period of the remainder [period / (from the timing of f up to the timing of m) / in an one frame period / about 2 field] in reversed polarity will become like-pole nature (from the timing of 1 f-f, and the timing of m to 4f termination). Therefore, the sum total of the period used as the reversed polarity in the scanning line of the both sides which adjoin to every scanning line becomes almost equal to 3 field period (1 field period of 2 field period with an upside, and the bottom). (However, in the 1f of the 1 field periods of a frame period first [each], about the gate line by which a polarity is chosen by changing by interlaced scanning) The period to timing when writing is performed from initiation of 1f of 1 field periods to a gate line just before [that] adjoining, or the period when only the part of the difference of the period to timing when writing is performed from initiation of 1f of 1 field periods, and the period to timing when writing is performed from initiation of 1f of 1 field periods in front of 1 selection period serves as reversed polarity becomes large slightly.

Thus, since the period of the remainder [period / in the electrical potential difference which impresses the electrical potential difference impressed to each pixel on each gate line to each pixel of the adjacent upper and lower sides, and an one frame period / the about 1 field period or 2 field period] in reversed polarity can be made into like-pole nature, generating of a disclination line can be reduced, improvement in contrast and improvement in brightness can be attained, and it can improve image quality substantially.

[0068] The difference from an example 1 is the point of replacing the line chosen by 2f and 3f of the four field periods. CHIRATSUKI can be reduced by doing in this way.

[0069] In addition, as shown in drawing 5 (a), it explained by the approach of impressing an electrical potential difference to each pixel, but even if it reverses a polarity for every source line, or the above-mentioned example reverses a polarity for every two source lines as shown in drawing 5 (c) as shown in drawing 5 (b), it can be driven by the same approach.

[0070] (Example 4) This example is the same actuation approach as an example 3, and is the actuation approach at the time of changing the number of the field periods divided at an one-frame period, and making it 8 field period.

[0071] The polarity of the electrical potential difference impressed to the pixel of the direction of the scanning line as drawing 4 is shown in drawing 5 (a) by the case of being the same In drawing showing the polarity of the electrical potential difference impressed to each pixel in the case of dividing into the 8 fields and driving, and the timing of electrical-potential-difference writing Y1-Yn of drawing 4 are drawing showing the timing which is turning on and writing in the polarity of an electrical potential difference and the transistor of each pixel which are impressed to each pixel on each gate line of Y1-Yn of drawing 6 (b). The polarity of the electrical potential difference impressed to each pixel is the common electrode 608 (the common electrode 608 shows the transparent electrode 73 of drawing 7 .) of drawing 6 . It expresses with forward and negative on the basis of potential. Moreover, drawing shown by drawing 4 expresses the polarity of the electrical potential difference impressed to each pixel, and does not express the voltage level impressed actually. According to an indicative data, as for the electrical potential difference actually impressed to each pixel, a different electrical potential difference of a voltage level is impressed.

[0072] In 1F of drawing 4 , 2F express the 2nd frame with the 1st frame.

[0073] With the 1st frame, first, the gate lines Y1 and Y9, ..., Yn-7, and interlaced scanning in every eight lines are performed, selection is made and writing is performed in the 1st field shown by 1f. Writing is performed with straight polarity and, as for Y1, Y17, ..., Yn-7 (gate line which corresponds every 16 lines from Y1), writing is performed by negative polarity, as for Y9, Y25, and ... (gate line which corresponds every 16 lines from Y9). It holds to the timing of a' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y1 between one selection periods to the timing of a, and is written in a degree. And in the next selection period, it holds to the timing of b' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y9 between one selection periods to the timing of b, and is written in a degree. Thus, it holds until make sequential selection, it goes by interlaced scanning in every eight lines, an electrical potential difference is written in to each pixel on gate line Yn-7 and it is written in a degree, reversing the polarity of a write-in electrical potential difference. The 2nd field which 1 field period ends now and is shown by the following 2f is started.

[0074] In the 2nd field, the gate lines Y3 and Y11, ..., Yn-5, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y3, Y19, ..., Yn-5 (gate line which corresponds every 16 lines from Y3), writing is performed by negative polarity, as for

Y11, Y27, and ... (gate line which corresponds every 16 lines from Y11). It holds to the timing of c' of the 2nd frame which the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y3 between one selection periods to the timing of c, and is written in a degree. And in the next selection period, it holds to the timing which was late for c' of the 2nd frame which the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y11 between one selection periods to the timing which was late for c during the 1 selection, and is written in a degree during the 1 selection. Thus, it holds until make sequential selection, it goes by interlaced scanning in every eight lines, an electrical potential difference is written in to each pixel on gate line Yn-5 and it is written in a degree, reversing the polarity of a write-in electrical potential difference. The 3rd field which 2 field period ends now and is shown by the following 3f is started.

[0075] In the 3rd field, the gate lines Y2 and Y10, ..., Yn-6, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y2, Y18, ..., Yn-6 (gate line which corresponds every 16 lines from Y2), writing is performed by negative polarity, as for Y10, Y26, and ... (gate line which corresponds every 16 lines from Y10). It holds until the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y2 between one selection periods to the timing of d and it is written in a degree. And in the next selection period, it holds until the electrical potential difference by the side of negative polarity is written in the pixel on the gate line Y10 between one selection periods to the timing of e and it is written in a degree. Thus, it holds until it writes in every eight lines, and make sequential selection, it goes, an electrical potential difference is written in to each pixel on gate line Yn-6 and it is written in a degree, reversing the polarity of an electrical potential difference. The 4th field which 3 field period ends now and is shown by the following 4f starts.

[0076] Thus, in the 4th field, the gate lines Y4 and Y12, ..., Yn-4, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y4, Y20, ..., Yn-4 (gate line which corresponds every 16 lines from Y4), writing is performed by negative polarity, as for Y12, Y28, and ... (gate line which corresponds every 16 lines from Y12). It holds until the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y4 between one selection periods to the timing of f and it is written in a degree. And a gate line is chosen every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.

[0077] In the 5th field, the gate lines Y5 and Y13, ..., Yn-3, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y5, Y21, ..., Yn-3 (gate line which corresponds every 16 lines from Y5), writing is performed by negative polarity, as for Y13, Y29, and ... (gate line which corresponds every 16 lines from Y13). It holds until the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y5 between one selection periods to the timing of g and it is written in a degree. And a gate line is chosen every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.

[0078] In the 6th field, the gate lines Y7 and Y15, ..., Yn-1, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y7, Y23, ..., Yn-1 (gate line which corresponds every 16 lines from Y7), writing is performed by negative polarity, as for Y15, Y31, and ... (gate line which corresponds every 16 lines from Y15). It holds until the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y7 between one selection periods to the timing of h and it is written in a degree. And a gate line is chosen every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.

[0079] In the 7th field, the gate lines Y6 and Y14, ..., Yn-2, and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y6, Y22, ..., Yn-2 (gate line which corresponds every 16 lines from Y6), writing is performed by negative polarity, as for Y14, Y30, and ... (gate line which corresponds every 16 lines from Y14). It holds until the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y6 between one selection periods to the

timing of i and it is written in a degree. And a gate line is chosen every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.

[0080] In the 8th field, the gate lines Y8, Y16, ..., Yn and interlaced scanning in every eight lines are performed, selection is made and writing is performed. Writing is performed with straight polarity and, as for Y8, Y24, ..., Yn (gate line which corresponds every 16 lines from Y8), writing is performed by negative polarity, as for Y16, Y32, and ... (gate line which corresponds every 16 lines from Y16). It holds until the electrical potential difference by the side of straight polarity is written in the pixel on the gate line Y8 between one selection periods to the timing of j and it is written in a degree. And a gate line is chosen every eight lines, and changing the polarity of the electrical potential difference impressed to each pixel for every selection period, it holds until an electrical potential difference is written in each pixel on the selected gate line and it is written in a degree.

[0081] Thus, it ends to the 8th field, the 1st frame is completed, and then the 2nd frame is started.

[0082] He is trying for the 2nd frame to write an electrical potential difference in each pixel with the 1st frame and reversed polarity in the same way as the 1st frame. And this actuation is repeated and alternating current actuation of each pixel is carried out.

[0083] The electrical potential difference impressed to the source line shown by X1-Xm by carrying out such actuation, changing a polarity for every selection period For example, the applied voltage of each pixel on the gate line Y2 of drawing 6 (b) is received. If the electrical potential difference currently impressed to each pixel on the gate line Y1 on it is seen about the 1st frame period of drawing 4 , the period (3f-8f) of the remainder [period / (1f-2f) / in an one frame period / about 2 field] in reversed polarity will become like-pole nature. And if the electrical potential difference currently impressed to each pixel on the gate line Y3 under it is seen about the 1st frame period of drawing 4 to the applied voltage of each pixel on the gate line Y2, the period (1f and 3f-8f) of the remainder [period / (2f) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature.

[0084] Moreover, if the electrical potential difference currently impressed to each pixel on the gate line Y6 on it is seen about the 1st frame period of drawing 4 to the applied voltage of each pixel on the gate line Y7 of drawing 6 (b), the period (1f-5f, and 7f-8f) of the remainder [period / (6f) / in an one frame period / about 1 field] in reversed polarity will become like-pole nature. And if the electrical potential difference currently impressed to each pixel on the gate line Y8 under it is seen about the 1st frame period of drawing 4 to the applied voltage of each pixel on the gate line Y7, the period (1f-5f, and 8f) of the remainder [period / (6f-7f) / in an one frame period / about 2 field] in reversed polarity will become like-pole nature. Therefore, the sum total of the period used as the reversed polarity in the scanning line of the both sides which adjoin to every scanning line becomes almost equal to 3 field period (1 field period of 2 field period with an upside, and the bottom). (However, in the 1f of the 1 field periods of a frame period first [each], about the gate line by which a polarity is chosen by changing by interlaced scanning) The period to timing when writing is performed from initiation of 1f of 1 field periods to a gate line just before [that] adjoining, or the period when only the part of the difference of the period to timing when writing is performed from initiation of 1f of 1 field periods, and the period to timing when writing is performed from initiation of 1f of 1 field periods in front of 1 selection period serves as reversed polarity becomes large slightly.

Thus, since the period of the remainder [period / in the electrical potential difference which impresses the electrical potential difference impressed to each pixel on each gate line to each pixel of the adjacent upper and lower sides, and an one frame period / the about 1 field period or 2 field period] in reversed polarity can be made into like-pole nature, generating of a disclination line can be reduced, improvement in contrast and improvement in brightness can be attained, and it can improve image quality substantially. Moreover, CHIRATSUKI can be reduced.

[0085] In addition, as shown in drawing 5 (a), it explained by the approach of impressing an electrical potential difference to each pixel, but even if it reverses a polarity for every source line, or the above-mentioned example reverses a polarity for every two source lines as shown in drawing 5 (c) as shown in drawing 5 (b), it can be driven by the same approach. (Although 4 pixels of polarities have reversed drawing 5 at a time in the direction of a gate line since it shows the case where divide an one-frame period into the 4 fields, and it is driven as shown in an example 3) this changes to every 8 pixels polarity reversals in the example 4. (Example 5) If even the about 32 field is divided when the actuation approach shown in the above-mentioned examples 1-4 estimates display quality, changing the number of the fields divided at an one-frame period The effect of

disclination was lost mostly and it has checked that lowering of brightness or contrast was canceled.

[0086] Moreover, the control circuit of a liquid crystal display will become so complicated that the number of the fields to divide increases.

[0087] The number of the fields divided from these things was making it the range of 2-32, and optimization of a control circuit was also realizable, realizing improvement in display quality, such as brightness and contrast.

[0088] (Example 6) When the liquid crystal projector using the liquid crystal light valve of the reflective mold by the actuation approach shown in the above and examples 1-5 was produced and carried out and image quality was evaluated, brightness and contrast improved and image quality went up substantially.

[0089] Moreover, when the liquid crystal display of the direct viewing type using an amorphous silicon TFT was produced and image quality was evaluated, brightness and contrast improved and image quality went up. By building this indicating equipment into a personal computer or television, image quality can improve and legible electronic equipment can be offered.

[0090] In addition, although the case where examples 1, 2, 3, 4, and 6 divided an one-frame period into the 4 fields and the 8 field was explained as an example, the number of the fields to divide should just be an integer below the number of scanning lines or more in two. Moreover, it may be made an integral multiple including the scanning line of imagination, and if it finishes choosing the scanning line of the last chosen for every field, you may make it go to the next field, even when the number of scanning lines does not become the integral multiple of the number of the fields.

[0091] moreover, even if it sets to obtain with 45-degree twist TN mode, the objects, for example, TN mode, other than the liquid crystal mode shown in the examples 1-6, by the same actuation approach, a disclination line can be reduced and image quality can be improved.

[0092] Moreover, although the liquid crystal light valve of the reflective mold which included the liquid crystal driver in the silicon substrate, and attached the switching element by the MOS transistor to each pixel was made into the example and examples 1-6 explained it, if it is the liquid crystal display of the active matrix by switching elements, such as an amorphous silicon TFT and poly-Si TFT, a disclination line can be reduced by the same actuation approach, and image quality can be improved. Moreover, it can drive by the view with the same said of the liquid crystal display of the active matrix using nonlinear 2 terminal component.

[0093]

[Effect of the Invention] As stated above, according to the liquid crystal display of this invention, the period of the electrical potential difference impressed to each pixel of the upper and lower sides which the electrical potential difference impressed to each pixel on each gate line adjoins, and reversed polarity only in the part in the whole period which is impressing the electrical potential difference Since the die length of the period when the remaining periods can be made into like-pole nature at, and the electrical potential difference of reversed polarity is impressed is made almost similarly about every line Generating of a disclination line can be reduced, improvement in contrast and improvement in brightness can be attained, CHIRATSUKI can also be reduced, and image quality can be improved substantially.

[0094] Moreover, brightness and contrast of electronic equipment of this invention improve, CHIRATSUKI can be reduced, and its image quality of a liquid crystal display can improve substantially, and it can be made legible.

[Brief Description of the Drawings]

[Drawing 1] Drawing showing the polarity of the electrical potential difference impressed to each pixel in the one example of this invention, and the timing of electrical-potential-difference writing.

[Drawing 2] Drawing showing the polarity of the electrical potential difference impressed to each pixel in the one example of this invention, and the timing of electrical-potential-difference writing.

[Drawing 3] Drawing showing the polarity of the electrical potential difference impressed to each pixel in the one example of this invention, and the timing of electrical-potential-difference writing.

[Drawing 4] Drawing showing the polarity of the electrical potential difference impressed to each pixel in the one example of this invention, and the timing of electrical-potential-difference writing.

[Drawing 5] Drawing showing the polarity of the electrical potential difference impressed to each pixel in the one example of this invention at the 1st frame period.

[Drawing 6] The block diagram showing the actuation circuit of an active matrix liquid crystal indicating equipment, and an example of the configuration of a pixel.

[Drawing 7] The sectional view showing an example of the configuration of a high-reflective-liquid-crystal light valve.

[Drawing 8] Drawing showing the situation of generating of a disclination line.

[Drawing 9] Drawing showing the polarity of the electrical potential difference conventionally

impressed to each pixel in actuation.

[Description of Notations]

601. Equal Circuit of Pixel Section
602. Transistor
603. Gate
604. Source
605. Drain and Pixel Electrode
606. Liquid Crystal
607. Retention Volume
608. Common electrode
611. Signal-Line Driver
612. Gate Line Driver
613. Pixel Section
614. Gate Line
615. Source line
71. Polarization Means
72. Glass Substrate
73. Transparent Electrode
74.76. Orientation Film
75. Liquid Crystal
77. Silicon Substrate

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（A）**　(11)特許出願公開番号

特開平11－295697

(43)公開日　平成11年(1999)10月29日

(51)Int.Cl.[6]		識別記号	FI		
Ｇ０２Ｆ	1/133	５５０	Ｇ０２Ｆ	1/133	５５０
Ｇ０９Ｇ	3/36		Ｇ０９Ｇ	3/36	
Ｈ０４Ｎ	5/66	１０２	Ｈ０４Ｎ	5/66	１０２Ｂ

審査請求　未請求　請求項の数８　ＯＬ　（全 14 頁）

(21)出願番号　特願平10－105226

(22)出願日　平成10年(1998)４月15日

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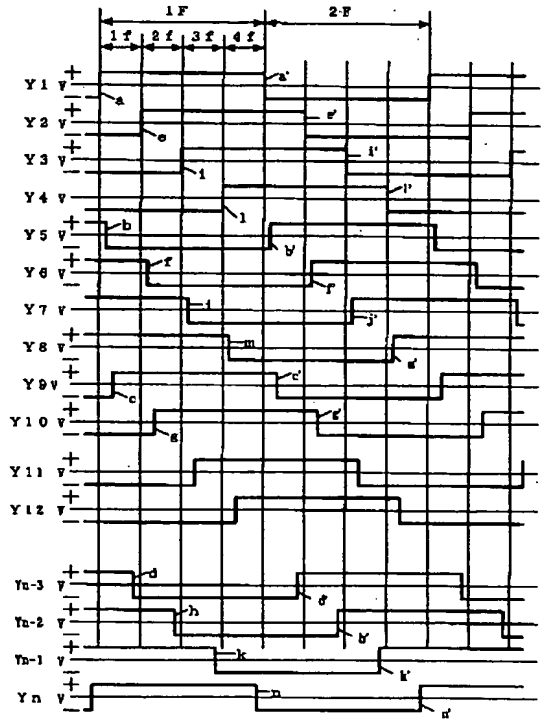
(54)【発明の名称】　液晶表示装置の駆動方法及び電子機器

(57)【要約】

【課題】隣接する画素間で印加電圧の極性の違いによって発生する、ディスクリネーションラインの発生を防止する。

【解決手段】１フレーム期間を複数のフィールドに分け、各フィールドごとに何ラインか飛越しながら１選択期間ごとに印加電圧の極性を反転していく事によって、隣接する各画素に印加している電圧の極性が逆になる時間を短くする事で、ディスクリネーションラインの発生を低減する事ができる。



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【特許請求の範囲】

【請求項１】　各画素にスイッチング素子を設けたアクティブマトリクス型の液晶表示装置において、第１の走査線上の各画素に印加する電圧の極性は、１フレーム期間において前記第１の走査線と隣接する走査線上の各画素に印加する電圧の極性に対して、共通電極の電位を基準に逆極性となる第１の期間と同極性となる第２の期間とを有することを特徴とする液晶表示装置の駆動方法。

【請求項２】　第１の走査線上の各画素に印加する電圧と、第１の走査線の両側の走査線上の各画素に印加する電圧とを比較し、前記第１の期間の合計がどの走査線に対してもほぼ同じになることを特徴とする請求項１記載の液晶表示装置の駆動方法。

【請求項３】　１フレーム期間をＮ（Ｎは２以上の整数）個のサブ期間に分け、各サブ期間はＮ走査線ごとに飛越しながら１走査期間ごとに印加電圧の極性を反転させることを特徴とする請求項１乃至２記載の液晶表示装置の駆動方法。

【請求項４】　１フレーム期間をＮ（２≦Ｎ≦３２の整数）個のサブ期間に分け、各サブ期間はＮ走査線ごとに飛越しながら１走査期間ごとに印加電圧の極性を反転させることを特徴とする請求項３記載の液晶表示装置の駆動方法。

【請求項５】　前記サブ選択期間ごとに走査する走査線の順番を入れ替えることを特徴とする請求項３記載の液晶表示装置の駆動方法。

【請求項６】　同一走査線上の各画素に印加する電圧の極性が同じであることを特徴とする請求項１から５記載の液晶表示装置の駆動方法。

【請求項７】　同一走査線上の各画素に印加する電圧の極性は１画素ごとあるいは２画素ごとに共通電極の電位を基準として逆極性であることを特徴とする請求項１から５記載の液晶表示装置の駆動方法。

【請求項８】　請求項１から７記載の駆動方法を用いた液晶表示装置を備えたことを特徴とする電子機器。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、液晶表示装置の駆動方法に関するもので、特に、アクティブマトリクス方式の液晶表示装置の駆動方法に関するものである。また、アクティブマトリクス方式の液晶表示装置の駆動方法を用いた液晶表示装置とその液晶表示装置を備えた電子機器に関するものである。

【０００２】

【従来の技術】従来のアクティブマトリクスの液晶表示装置の駆動方法として、特公平５－２９９１６に記載されているような駆動方法がある。

【０００３】この駆動方法は、図９の（ａ）で示すように１走査線ごとに各画素に印加する電圧の極性を逆にする方法や、（ｂ）で示すように各画素に印加する電圧の極性が隣どうしで逆にする等の駆動方法である。この駆動方法は、画面のチラツキの防止や表示ムラの改善等を主な目的としている。

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【０００４】

【発明が解決しようとする課題】このような駆動方法の場合、隣どうしの画素に印加される電圧が、１フレーム期間のほとんどの期間で逆極性となってしまうために図８に示すように、隣どうしの画素に印加する電圧の極性が逆の場合ディスクリネーションラインが発生してしまう。

【０００５】例えば、図７に示す反射型液晶ライトバルブの構成で、７１が偏光手段、７２がガラス基板、７３が透明電極、７４が配向膜、７５が液晶、７６が配向膜、７７がシリコン基板で、このシリコン基板７７上に図６に示すような回路が構成され、液晶７５は傾斜垂直配向セルに誘電率異方性が負のネマチック液晶を入れて、液晶に電圧を印加しない状態の時に暗くなる液晶モードの場合を例にして説明する。

【０００６】各画素にオン電圧を印加して白表示して、隣どうしの画素に印加する電圧の極性が逆の場合に発生するディスクリネーションラインは暗くなる。このディスクリネーションライン発生の様子を図８に示す。８１～８４は各画素を表し、＋、－は各画素に印加している電圧の極性を表している。そして、８５～８８が各画素に発生するディスクリネーションラインの発生の様子を表している。このように、各画素の境界線付近に暗いディスクリネーションラインが発生してしまう。このディスクリネーションラインは、コントラストの低下や輝度の低下といった画質低下の原因となってしまう。

【０００７】そして、最近のように高精細化が進み１画素のサイズが小さくなると、画素面積に対するディスクリネーションラインの発生面積の割合が増え、画質の低下がより深刻になる。

【０００８】特に、液晶プロジェクタ等に使うライトバルブ等は画面サイズが小さく、高精細化が要求されているためによけいに影響を受けやすい。その中でも、特開平９－２３６８１４に示されているような反射型の液晶ライトバルブの場合、各画素間の隙間が小さく、しかも画素サイズも小さいためにディスクリネーションラインの影響が大きく、画質も低下してしまう。

【０００９】また、ディスクリネーションラインを発生させないためにすべての画素に印加する電圧の極性を同じにして、フレームごとの極性の反転だけをすることもできるがチラツキが発生してしまう。

【００１０】

【課題を解決するための手段】請求項１記載の液晶表示装置は、各画素にスイッチング素子を設けたアクティブマトリクス型の液晶表示装置において、第１の走査線上の各画素に印加する電圧の極性は、１フレーム期間において前記第１の走査線と隣接する走査線上の各画素に印

加する電圧の極性に対して、共通電極の電位を基準に逆極性となる第１の期間と同極性となる第２の期間とを有することを特徴とする。

【００１１】上記の構成によれば、隣接する画素に印加する電圧の極性が逆の場合に発生するディスクリネーションラインの発生を低減でき、液晶表示装置の輝度やコントラストを向上できるという効果を有する。

【００１２】請求項２記載の液晶表示装置は、第１の走査線上の各画素に印加する電圧と、第１の走査線の両側の走査線上の各画素に印加する電圧とを比較し、前記第１の期間の合計がどの走査線に対してもほぼ同じになることを特徴とする。

【００１３】上記の構成によれば、隣接する画素に印加する電圧の極性が逆の場合に発生するディスクリネーションラインの発生を低減でき、液晶表示装置の輝度やコントラストを向上できるという効果を有する。

【００１４】請求項３記載の液晶表示装置は、１フレーム期間をＮ（Ｎは２以上の整数）個のサブ期間に分け、各サブ期間はＮ走査線ごとに飛越しながら１走査期間ごとに印加電圧の極性を反転させることを特徴とする。

【００１５】上記の構成によれば、隣接する画素に印加する電圧の極性が逆の場合に発生するディスクリネーションラインの発生を低減でき、液晶表示装置の輝度やコントラストを向上できるという効果を有する。

【００１６】請求項４記載の液晶表示装置は、１フレーム期間をＮ（２≦Ｎ≦３２の整数）個のサブ期間に分け、各サブ期間はＮ走査線ごとに飛越しながら１走査期間ごとに印加電圧の極性を反転させることを特徴とする。

【００１７】上記の構成によれば、隣接する画素に印加する電圧の極性が逆の場合に発生するディスクリネーションラインの発生を低減でき、液晶表示装置の輝度やコントラストを向上でき、制御回路の最適化もできるという効果を有する。

【００１８】請求項５記載の液晶表示装置は、前記サブ選択期間ごとに走査する走査線の順番を入れ替えることを特徴とする。

【００１９】上記の構成によれば、隣接する画素に印加する電圧の極性が逆の場合に発生するディスクリネーションラインの発生を低減でき、液晶表示装置の輝度やコントラストを向上でき、チラツキの低減もできるという効果を有する。

【００２０】請求項６記載の液晶表示装置は、同一走査線上の各画素に印加する電圧の極性が同じであることを特徴とする。

【００２１】上記の構成によれば、隣接する画素に印加する電圧の極性が逆の場合に発生するディスクリネーションラインの発生を低減でき、液晶表示装置の輝度やコントラストを向上できるという効果を有する。

【００２２】請求項７記載の液晶表示装置は、同一走査線上の各画素に印加する電圧の極性は１画素ごとあるいは２画素ごとに共通電極の電位を基準として逆極性であることを特徴とする。

【００２３】上記の構成によれば、隣接する画素に印加する電圧の極性が逆の場合に発生するディスクリネーションラインの発生を低減でき、液晶表示装置の輝度やコントラストを向上でき、チラツキの低減もできるという効果を有する。

【００２４】請求項８記載の電子機器は、請求項１から７記載の駆動方法を用いた液晶表示装置を備えたことを特徴とする。

【００２５】上記構成によれば、明るくて、コントラストが高く、見やすく、表示品質の高い電子機器を提供できるという効果を有する。

【００２６】

【発明の実施の形態】以下、本発明の実施形態を図面に基づいて説明する。

【００２７】尚、本実施例１から６は、図６に示すように各画素にトランジスタを設けたアクティブマトリクスで、図７に示す反射型液晶ライトバルブを例に上げて説明する。

【００２８】図６（ａ）の６０１は画素部の等価回路の一例を示す図で、６０２がトランジスタで、６０３がトランジスタのゲート、６０４がトランジスタのソース、６０５がトランジスタのドレイン及び画素電極、６０６が液晶、６０７が保持容量、６０８が共通電極、をそれぞれ示している。そして、（ｂ）がアクティブマトリクス型液晶表示装置の駆動回路の一例のブロック図で、６１１が信号線ドライバ、６１２がゲート線ドライバ、Ｙ１～Ｙｎがゲート線、Ｘ１～Ｘｍがソース線、をそれぞれ示している。

【００２９】そして、図６（ｂ）に示すように、６０１で示す各画素のゲート６０３がゲート線とつながりソース６０４がソース線とつながっている。

【００３０】また、図７は反射型液晶ライトバルブの構成の一例を示す図で、７１が偏光手段、７２がガラス基板、７３が透明電極、７４が配向膜、７５が液晶、７６が配向膜、７７がシリコン基板で、このシリコン基板７７上に図６に示すような回路が構成されている。そして、液晶７５は傾斜垂直配向セルに誘電率異方性が負のネマチック液晶を入れ、液晶に電圧を印加しない状態の時に暗くなる液晶モードの場合を例にして説明する。

【００３１】（実施例１）図１は、図５（ａ）に示される表示の各走査線方向の画素に電圧が書き込まれるタイミングと電圧の極性を示すものである。走査線方向の画素に印加される電圧の極性は同じ場合で、４フィールドに分けて駆動をおこない、図１のＹ１～Ｙｎは図６（ｂ）のＹ１～Ｙｎの各ゲート線上の各画素のトランジスタをオンして書き込んでいるタイミングと１選択期間に書き込みが行われた後に引き続きそのままの極性で電

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圧が保持されている状態を示している。各画素に印加する電圧の極性は図６の共通電極６０８（共通電極６０８は図７の透明電極７３を示す。）の電位Ｖを基準にして正、負で表している。

【００３２】図１の１Ｆは第１のフレームで２Ｆは第２のフレームを表している。

【００３３】第１のフレームでは、まず、１ｆで示す第１フィールドで、ゲート線Ｙ１、Ｙ５、Ｙ９、...Yn-3と４ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ１、Ｙ９、･･･（Ｙ１から８ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ５、･･･、Yn-3（Ｙ５から８ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ１上の画素にａのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのａ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ５上の画素にｂのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｂ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ９上の画素にｃのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれ第２のフレームのｃ’のタイミングるまで保持する。このように、書き込み電圧の極性を反転させながら４ライン毎の飛越し走査で順次選択して行き、ゲート線Yn-3にｄのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｄ’のタイミングまで保持する。これで１フィールド期間（１ｆ）が終了して、次の２ｆで示す第２フィールドが開始される。

【００３４】第２フィールドでは、ゲート線Ｙ２、Ｙ６、Ｙ１０、...Yn-2と４ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ２、Ｙ１０、･･･（Ｙ２から８ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ６、･･･、Yn-2（Ｙ６から８ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ２上の画素にｅのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｅ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ６上の画素にｆのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｆ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ１０上の画素にｇのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｇ’のタイミングまで保持する。このように、書き込み電圧の極性を反転させながら４ライン毎の飛越し走査で順次選択して行き、ゲート線Yn-2にｈのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｈ’のタイミングまで保持する。これで２フィールド期間が終了

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して、次の３ｆで示す第３フィールドが始まる。

【００３５】第３フィールドでは、ゲート線Ｙ３、Ｙ７、Ｙ１１、...、Yn-1と４ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ３、Ｙ１１、･･･（Ｙ３から８ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ７、･･･、Yn-1（Ｙ７から８ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ３上の画素にｉのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｉ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ７上の画素にｊのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｊ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ１１上の画素にｊから１選択期間遅れたタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｊ’から1選択期間遅れたタイミングまで保持する。このように、書き込み電圧の極性を反転させながら４ライン毎の飛越し走査で順次選択して行き、ゲート線Yn-1にｋのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｋ’のタイミングまで保持する。これで３フィールド期間が終了して、次の４ｆで示す第４フィールドが開始される。

【００３６】第４フィールドでは、ゲート線Ｙ４、Ｙ８、Ｙ１２...、Ynと４ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ４、Ｙ１２、･･･（Ｙ４から８ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ８、･･･、Yn（Ｙ８から８ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ４上の画素にｌのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｌ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ８上の画素にｍのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｍ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ１２上の画素にｍから１選択期間遅れたタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｍ’から１選択期間遅れたタイミングまで保持する。このように、書き込み電圧の極性を反転しながら４ライン毎の飛越し走査で順次選択して行き、ゲート線Ynにｎのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｎ’のタイミングまで保持する。これで４フィールド期間が終了して、第１のフレームが終了して、次に第２のフレームが開始される。

【００３７】第２のフレームは、第１のフレームと同じ要領で第１のフレームと逆極性で各画素に電圧を書き込むようにしている。そして、この動作を繰り返し、各画

素が交流駆動される。

【００３８】このような駆動をする事によって、Ｘ１～Ｘｍで示すソース線に印加する電圧は１選択期間毎に極性を切替えながら、例えば、図６（ｂ）のゲート線Ｙ２上の各画素の印加電圧に対して、その上のゲート線Ｙ１上の各画素に印加されている電圧は図１の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（１ｆ）だけが逆極性で残りの期間（２ｆ～４ｆ）は同極性になる。そして、ゲート線Ｙ２上の各画素の印加電圧に対して、その下のゲート線Ｙ３上の各画素に印加されている電圧は図１の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（２ｆ）だけが逆極性で残りの期間（１ｆと３ｆ～４ｆ）は同極性になる。

【００３９】また、図６（ｂ）のゲート線Ｙ７上の各画素の印加電圧に対して、その上のゲート線Ｙ６上の各画素に印加されている電圧は図１の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（ｆのタイミングからｊのタイミングまで）だけが逆極性で残りの期間（１ｆからｆのタイミングとｊのタイミングから４ｆの終了まで）は同極性になる。そして、その下のゲート線Ｙ８上の各画素に印加されている電圧は図１の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（ｊのタイミングからｍのタイミングまで）だけが逆極性で残りの期間（１ｆからｊのタイミングとｍのタイミングから４ｆの終了まで）は同極性になる。従って、どの走査線に対しても隣接する両側の走査線での逆極性となる期間の合計は２フィールド期間（上下両側での各１フィールド期間ずつ）とほぼ等しくなる。（但し、各フレーム期間始めの１フィールド期間１ｆにおいて、飛び越し走査で極性が切り替わって選択されるゲート線については、隣接するその直前のゲート線に対して、１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間、或いは１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間と１選択期間前の１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間との差の分だけ、逆極性となる期間が僅かに大きくなる。）

このように、各ゲート線上の各画素に印加する電圧は隣り合う上下の各画素に印加する電圧と１フレーム期間中のほぼ１フィールド期間だけが逆極性で残りの期間は同極性とする事ができるために、ディスクリネーションラインの発生を低減する事ができ、コントラストの向上、輝度の向上が可能になり、画質を大幅に向上する事ができる。

【００４０】尚、上記実施例は図５（ａ）に示すように各画素に電圧を印加する方法で説明したが、図５（ｂ）に示すようにソース線ごとに極性を反転したり、図５（ｃ）に示すようにソース線２本ごとに極性を反転しても同様の方法で駆動する事ができる。

【００４１】また、図１で示す図は、各画素に印加する電圧の極性を表すもので、実際に印加される電圧レベルを表すものではない。実際に各画素に印加する電圧は表示データに合わせて電圧レベルの異なる電圧が印加される。

【００４２】（実施例２）本実施例は、実施例１と同様の駆動方法で、１フレーム期間に分割するフィールド期間の数を変えて８フィールド期間にした場合の駆動方法である。

【００４３】図２は、図５（ａ）に示される表示の各走査線方向の画素に電圧が書き込まれるタイミングと電圧の極性を示すものである。走査線方向の画素に印加する電圧の極性は同じ場合で、８フィールドに分けて駆動をおこない、図２のＹ１～Ｙｎは図６（ｂ）のＹ１～Ｙｎの各ゲート線上の各画素のトランジスタをオンして書き込んでいるタイミングと１選択期間に書き込みが行われた後に引き続きそのままの極性で電圧が保持されている状態を示している。各画素に印加する電圧の極性は図６の共通電極６０８（共通電極６０８は図７の透明電極７３を示す。）の電位Ｖを基準にして正、負で表している。

【００４４】図２の１Ｆは第１のフレームで２Ｆは第２のフレームを表している。

【００４５】第１のフレームでは、まず、１ｆで示す第１フィールドで、ゲート線Ｙ１、Ｙ９、...、Yn-7と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ１、Ｙ１７、･･･、Yn-7（Ｙ１から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ９、Ｙ２５、･･･（Ｙ９から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ１上の画素にａのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのａ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ９上の画素にｂのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｂ’のタイミングまで保持する。このように、書き込み電圧の極性を反転させながら８ライン毎の飛び越し走査で順次選択して行き、ゲート線Yn-7上の各画素まで電圧が書き込まれて次に書き込まれるまで保持する。これで１フィールド期間が終了して、次の２ｆで示す第２フィールドが開始される。

【００４６】第２フィールドでは、ゲート線Ｙ２、Ｙ１０、...、Yn-6と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ２、Ｙ１８、･･･、Yn-6（Ｙ２から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１０、Ｙ２６、･･･（Ｙ１０から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ２上の画素にｃの

タイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｃ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ１０上の画素にｄのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｄ’のタイミングまで保持する。このように、書き込み電圧の極性を反転させながら８ライン毎の飛び越し走査で順次選択して行き、ゲート線Yn-6上の各画素まで電圧が書き込まれて次に書き込まれるまで保持する。これで２フィールド期間が終了して、次の３ｆで示す第３フィールドが開始される。

【００４７】このようにして、第３フィールドでは、ゲート線Ｙ３、Ｙ１１、...、Yn-5と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ３、Ｙ１９、･･･、Yn-5（Ｙ３から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１１、Ｙ２７、･･･（Ｙ１１から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ３上の画素にｅのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｅ’のタイミングまで保持する。そして、８ラインごとの飛び越し走査によりゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００４８】第４フィールドでは、ゲート線Ｙ４、Ｙ１２、...、Yn-4と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ４、Ｙ２０、･･･、Yn-4（Ｙ４から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１２、Ｙ２８、･･･（Ｙ１２から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ４上の画素にｆのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｆ’のタイミングまで保持する。そして、８ラインごとの飛び越し走査によりゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００４９】第５フィールドでは、ゲート線Ｙ５、Ｙ１３、...、Yn-3と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ５、Ｙ２１、･･･、Yn-3（Ｙ５から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１３、Ｙ２９、･･･（Ｙ１３から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ５上の画素にｇのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｇ’のタイミングまで保持する。そして、８ラインごとの飛び越し走査によりゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００５０】第６フィールドでは、ゲート線Ｙ６、Ｙ１４、...、Yn-2と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ６、Ｙ２２、･･･、Yn-2（Ｙ６から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１４、Ｙ３０、･･･（Ｙ１４から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ６上の画素にｈのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｈ’のタイミングまで保持する。そして、８ラインごとの飛び越し走査によりゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００５１】第７フィールドでは、ゲート線Ｙ７、Ｙ１５、...、Yn-1と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ７、Ｙ２３、･･･、Yn-1（Ｙ７から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１５、Ｙ３１、･･･（Ｙ１５から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ７上の画素にｉのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｉ’のタイミングまで保持する。そして、８ラインごとの飛び越し走査によりゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００５２】第８フィールドでは、ゲート線Ｙ８、Ｙ１６、...、Ynと８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ８、Ｙ２４、･･･、Yn（Ｙ８から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１６、Ｙ３２、･･･（Ｙ１６から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ８上の画素にｊのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｊ’のタイミングまで保持する。そして、８ラインごとの飛び越し走査によりゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００５３】このようにして第８フィールドまで終了して第１のフレームが終了して、次に第２のフレームが開始される。

【００５４】第２のフレームは、第１のフレームと同じ要領で第１のフレームと逆極性で各画素に電圧を書き込

むようにしている。そして、この動作を繰り返し、各画素が交流駆動される。

【００５５】このような駆動をする事によって、Ｘ１～Ｘｍで示すソース線に印加する電圧は１選択期間ごとに極性を切替えながら、例えば、図６（ｂ）のゲート線Ｙ２上の各画素の印加電圧に対して、その上のゲート線Ｙ１上の各画素に印加されている電圧は図２の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（１ｆ）だけが逆極性で残りの期間（２ｆ～８ｆ）は同極性になる。そして、ゲート線Ｙ２上の各画素の印加電圧に対して、その下のゲート線Ｙ３上の各画素に印加されている電圧は図２の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（２ｆ）だけが逆極性で残りの期間（１ｆと３ｆ～８ｆ）は同極性になる。

【００５６】また、図６（ｂ）のゲート線Ｙ７上の各画素の印加電圧に対して、その上のゲート線Ｙ６上の各画素に印加されている電圧は図２の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（６ｆ）だけが逆極性で残りの期間（１ｆ～５ｆと７ｆ～８ｆ）は同極性になる。そして、ゲート線Ｙ７上の各画素の印加電圧に対して、その下のゲート線Ｙ８上の各画素に印加されている電圧は図２の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（７ｆ）だけが逆極性で残りの期間（１ｆ～６ｆと８ｆ）は同極性になる。従って、どの走査線に対しても隣接する両側の走査線での逆極性となる期間の合計は２フィールド期間（上下両側での各１フィールド期間ずつ）とほぼ等しくなる。（但し、各フレーム期間始めの１フィールド期間１ｆにおいて、飛び越し走査で極性が切り替わって選択されるゲート線については、隣接するその直前のゲート線に対して、１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間、或いは１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間と１選択期間前の１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間との差の分だけ、逆極性となる期間が僅かに大きくなる。）

このように、各ゲート線上の各画素に印加する電圧は隣り合う上下の各画素に印加する電圧と１フレーム期間中のほぼ１フィールド期間だけが逆極性で残りの期間は同極性とする事ができるために、ディスクリネーションラインの発生を低減する事ができ、コントラストの向上、輝度の向上が可能になり、画質を大幅に向上する事ができる。

【００５７】尚、上記実施例は図５（ａ）に示すように各画素に電圧を印加する方法で説明したが、図５（ｂ）に示すようにソース線ごとに極性を反転したり、図５（ｃ）に示すようにソース線２本ごとに極性を反転しても同様の方法で駆動する事ができる。（図５は実施例１に示すように、１フレーム期間を４フィールドに分けて駆動する場合を示しているためにゲート線方向に４画素づつ極性が反転しているが、実施例２ではこれが８画素づつの極性反転に変わる。）

また、図２で示す図は実施例１の説明で用いた図１と同様、各画素に印加する電圧の極性を表すもので、実際に印加される電圧レベルを表すものではない。実際に各画素に印加する電圧は表示データに合わせて電圧レベルの異なる電圧が印加される。

【００５８】（実施例３）図３において実施例３に係る図を図３に示す。

【００５９】図３で示す図は実施例１、２の説明で用いた図１、２と同様、各画素に印加する電圧の極性を表すもので、実際に印加される電圧レベルを表すものではない。実際に各画素に印加する電圧は表示データに合わせて電圧レベルの異なる電圧が印加される。また、各画素に印加する電圧の極性は図６の共通電極６０８（共通電極６０８は図７の透明電極７３を示す。）の電位Ｖを基準にして正、負で表している。

【００６０】図３の１Ｆは第１のフレームで２Ｆは第２のフレームを表している。

【００６１】第１のフレームでは、まず、１ｆで示す第１フィールドで、ゲート線Ｙ１、Ｙ５、Ｙ９、...Ｙn-3と４ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ１、Ｙ９、･･･（Ｙ１から８ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ５、･･･、Ｙn-3（Ｙ５から８ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ１上の画素にａのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのａ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ５上の画素にｂのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｂ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ９上の画素にｃのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｃ’のタイミングまで保持する。このように、書き込み電圧の極性を反転させながら４ライン毎の飛び越し走査で順次選択して行き、ゲート線Ｙn-3にｄのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｄ’のタイミングまで保持する。これで１フィールド期間が終了して、次の２ｆで示す第２フィールドが開始される。

【００６２】第２フィールドでは、ゲート線Ｙ３、Ｙ７、Ｙ１１、...、Ｙn-1と４ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ３、Ｙ１１、･･･（Ｙ３から８ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ７、･･･、Ｙn-1（Ｙ７から８ライン毎に相当するゲート線）は負極性で書き込

みが行われる。ゲート線Ｙ３上の画素にｅのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｅ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ７上の画素にｆのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｆ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ１１上の画素にｆから１選択期間遅れたタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｆ’から１選択期間遅れたタイミングまで保持する。このように、４ラインごとに書き込み電圧の極性を反転しながら順次選択して行き、ゲート線Ｙn-1にgのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｇ’のタイミングまで保持する。これで２フィールド期間が終了して、次の３ｆで示す第３フィールドが開始される。

【００６３】第３フィールドでは、ゲート線Ｙ２、Ｙ６、Ｙ１０、...Ｙn-2と４ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ２、Ｙ１０、･･･（Ｙ２から８ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ６、･･･、Ｙn-2（Ｙ６から８ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ２上の画素にｈのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｈ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ６上の画素にｉのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｉ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ１０上の画素にｊのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｊ’のタイミングまで保持する。このように、書き込み電圧の極性を反転させながら４ライン毎の飛び越し走査で順次選択して行き、ゲート線Ｙn-2にｋのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｋ’のタイミングまで保持する。これで３フィールド期間が終了して、次の４ｆで示す第４フィールドが開始される。

【００６４】第４フィールドでは、ゲート線Ｙ４、Ｙ８、Ｙ１２...、Ｙnと４ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ４、Ｙ１２、･･･（Ｙ４から８ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ８、･･･、Ｙn（Ｙ８から８ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ４上の画素にｌのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｌ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ８上の画素にｍのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｍ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ１２上の画素にｍから１選択期間遅れたタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｍ’から１選択期間遅れたタイミングまで保持する。このように、書き込み電圧の極性を反転させながら４ライン毎の飛び越し走査で順次選択して行き、ゲート線Ｙnにｎのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｎ’のタイミングまで保持する。これで４フィールド期間が終了して、第１のフレームが終了して、次に第２のフレームが開始される。

【００６５】第２のフレームは、第１のフレームと同じ要領で第１のフレームと逆極性で各画素に電圧を書き込むようにしている。そして、この動作を繰り返し、各画素が交流駆動される。

【００６６】このような駆動をする事によって、Ｘ１～Ｘｍで示すソース線に印加する電圧は１選択期間ごとに極性を切替えながら、例えば、図６（ｂ）のゲート線Ｙ２上の各画素の印加電圧に対して、その上のゲート線Ｙ１上の各画素に印加されている電圧は図３の第１のフレーム期間について見ると、１フレーム期間中のほぼ２フィールド期間（１ｆ～２ｆ）だけが逆極性で残りの期間（３ｆ～４ｆ）は同極性になる。そして、ゲート線Ｙ２上の各画素の印加電圧に対して、その下のゲート線Ｙ３上の各画素に印加されている電圧は図３の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（２ｆ）だけが逆極性で残りの期間（１ｆと３ｆ～４ｆ）は同極性になる。

【００６７】また、図６（ｂ）のゲート線Ｙ７上の各画素の印加電圧に対して、その上のゲート線Ｙ６上の各画素に印加されている電圧は図３の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（ｆのタイミングからｉのタイミングまで）だけが逆極性で残りの期間（１ｆ～ｉのタイミングとｉのタイミングから４ｆの終了まで）は同極性になる。そして、その下のゲート線Ｙ８上の各画素に印加されている電圧は図３の第１のフレーム期間について見ると、１フレーム期間中のほぼ２フィールド期間（ｆのタイミングからｍのタイミングまで）だけが逆極性で残りの期間（１ｆ～ｆのタイミングとｍのタイミングから４ｆの終了まで）は同極性になる。従って、どの走査線に対しても隣接する両側の走査線での逆極性となる期間の合計は３フィールド期間（上側との２フィールド期間と下側との１フィールド期間）とほぼ等しくなる。（但し、各フレーム期間始めの１フィールド期間１ｆにおいて、飛び越し走査で極性が切り替わって選択されるゲート線については、隣接するその直前のゲート線に対して、１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間、或いは１フィールド期間１ｆの開始から書き込み

が行われるタイミングまでの期間と１選択期間前の１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間との差の分だけ、逆極性となる期間が僅かに大きくなる。）

このように、各ゲート線上の各画素に印加する電圧は隣り合う上下の各画素に印加する電圧と１フレーム期間中のほぼ１フィールド期間あるいは２フィールド期間だけが逆極性で残りの期間は同極性とする事ができるために、ディスクリネーションラインの発生を低減する事ができ、コントラストの向上、輝度の向上が可能になり、画質を大幅に向上する事ができる。

【００６８】実施例１との違いは、４つのフィールド期間の内の２ｆと３ｆで選択するラインを入れ替えている点である。このようにする事によって、チラツキの低減をする事ができる。

【００６９】尚、上記実施例は図５（ａ）に示すように各画素に電圧を印加する方法で説明したが、図５（ｂ）に示すようにソース線ごとに極性を反転したり、図５（ｃ）に示すようにソース線２本ごとに極性を反転しても同様の方法で駆動する事ができる。

【００７０】（実施例４）本実施例は、実施例３と同様の駆動方法で、１フレーム期間に分割するフィールド期間の数を変えて８フィールド期間にした場合の駆動方法である。

【００７１】図４は、図５（ａ）に示すように走査線方向の画素に印加する電圧の極性は同じ場合で、８フィールドに分けて駆動する場合の各画素に印加する電圧の極性と電圧書き込みのタイミングを示す図で、図４のＹ１～Ｙｎは図６（ｂ）のＹ１～Ｙｎの各ゲート線上の各画素に印加する電圧の極性と各画素のトランジスタをオンして書き込んでいるタイミングを示す図で、各画素に印加する電圧の極性は図６の共通電極６０８（共通電極６０８は図７の透明電極７３を示す。）の電位を基準にして正、負で表している。また、図４で示す図は、各画素に印加する電圧の極性を表すもので、実際に印加される電圧レベルを表すものではない。実際に各画素に印加する電圧は表示データに合わせて電圧レベルの異なる電圧が印加される。

【００７２】図４の１Ｆは第１のフレームで２Ｆは第２のフレームを表している。

【００７３】第１のフレームでは、まず、１ｆで示す第１フィールドで、ゲート線Ｙ１、Ｙ９、...、Yn-7と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ１、Ｙ１７、･･･、Yn-7（Ｙ１から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ９、Ｙ２５、･･･（Ｙ９から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ１上の画素にａのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのａ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ９上の画素にｂのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｂ’のタイミングまで保持する。このように、書き込み電圧の極性を反転させながら８ライン毎の飛び越し走査で順次選択して行き、ゲート線Yn-7上の各画素まで電圧が書き込まれて次に書き込まれるまで保持する。これで１フィールド期間が終了して、次の２ｆで示す第２フィールドが開始される。

【００７４】第２フィールドでは、ゲート線Ｙ３、Ｙ１１、...、Yn-5と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ３、Ｙ１９、･･･、Yn-5（Ｙ３から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１１、Ｙ２７、･･･（Ｙ１１から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ３上の画素にｃのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｃ’のタイミングまで保持する。そして、次の選択期間ではゲート線Ｙ１１上の画素にｃから１選択期間遅れたタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれる第２のフレームのｃ’から１選択期間遅れたタイミングまで保持する。このように、書き込み電圧の極性を反転させながら８ライン毎の飛び越し走査で順次選択して行き、ゲート線Yn-5上の各画素まで電圧が書き込まれて次に書き込まれるまで保持する。これで２フィールド期間が終了して、次の３ｆで示す第３フィールドが開始される。

【００７５】第３フィールドでは、ゲート線Ｙ２、Ｙ１０、...、Yn-6と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ２、Ｙ１８、･･･、Yn-6（Ｙ２から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１０、Ｙ２６、･･･（Ｙ１０から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ２上の画素にｄのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれるまで保持する。そして、次の選択期間ではゲート線Ｙ１０上の画素にｅのタイミングで１選択期間の間に負極性側の電圧が書き込まれて次に書き込まれるまで保持する。このように、８ラインごとに書き込み電圧の極性を反転しながら順次選択して行き、ゲート線Yn-6上の各画素まで電圧が書き込まれて次に書き込まれるまで保持する。これで３フィールド期間が終了して、次の４ｆで示す第４フィールドが始まる。

【００７６】このようにして、第４フィールドでは、ゲート線Ｙ４、Ｙ１２、...、Yn-4と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ４、Ｙ２０、･･･、Yn-4（Ｙ４から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１２、Ｙ２８、･･･（Ｙ１２から１６ライン毎に相当する

ゲート線）は負極性で書き込みが行われる。ゲート線Ｙ４上の画素にｆのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれるまで保持する。そして、８ラインごとにゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００７７】第５フィールドでは、ゲート線Ｙ５、Ｙ１３、...、Yn-3と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ５、Ｙ２１、・・・、Yn-3（Ｙ５から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１３、Ｙ２９、・・・（Ｙ１３から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ５上の画素にｇのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれるまで保持する。そして、８ラインごとにゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００７８】第６フィールドでは、ゲート線Ｙ７、Ｙ１５、...、Yn-1と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ７、Ｙ２３、・・・、Yn-1（Ｙ７から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１５、Ｙ３１、・・・（Ｙ１５から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ７上の画素にｈのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれるまで保持する。そして、８ラインごとにゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００７９】第７フィールドでは、ゲート線Ｙ６、Ｙ１４、...、Yn-2と８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ６、Ｙ２２、・・・、Yn-2（Ｙ６から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１４、Ｙ３０、・・・（Ｙ１４から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ６上の画素にｉのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれるまで保持する。そして、８ラインごとにゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００８０】第８フィールドでは、ゲート線Ｙ８、Ｙ１６、...、Ynと８ライン毎の飛越し走査が行われ、選択がなされて書き込みが行われる。Ｙ８、Ｙ２４、・・・、Yn（Ｙ８から１６ライン毎に相当するゲート線）は正極性で書き込みが行なわれ、Ｙ１６、Ｙ３２、・・・（Ｙ１６から１６ライン毎に相当するゲート線）は負極性で書き込みが行われる。ゲート線Ｙ８上の画素にｊのタイミングで１選択期間の間に正極性側の電圧が書き込まれて次に書き込まれるまで保持する。そして、８ラインごとにゲート線を選択して、１選択期間ごとに各画素に印加する電圧の極性を切替えながら、選択したゲート線上の各画素に電圧が書き込まれて次に書き込まれるまで保持する。

【００８１】このようにして第８フィールドまで終了して第１のフレームが終了して、次に第２のフレームが開始される。

【００８２】第２のフレームは、第１のフレームと同じ要領で第１のフレームと逆極性で各画素に電圧を書き込むようにしている。そして、この動作を繰り返し、各画素が交流駆動される。

【００８３】このような駆動をする事によって、Ｘ１～Ｘｍで示すソース線に印加する電圧は１選択期間ごとに極性を切替えながら、例えば、図６（ｂ）のゲート線Ｙ２上の各画素の印加電圧に対して、その上のゲート線Ｙ１上の各画素に印加されている電圧は図４の第１のフレーム期間について見ると、１フレーム期間中のほぼ２フィールド期間（１ｆ～２ｆ）だけが逆極性で残りの期間（３ｆ～８ｆ）は同極性になる。そして、ゲート線Ｙ２上の各画素の印加電圧に対して、その下のゲート線Ｙ３上の各画素に印加されている電圧は図４の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（２ｆ）だけが逆極性で残りの期間（１ｆと３ｆ～８ｆ）は同極性になる。

【００８４】また、図６（ｂ）のゲート線Ｙ７上の各画素の印加電圧に対して、その上のゲート線Ｙ６上の各画素に印加されている電圧は図４の第１のフレーム期間について見ると、１フレーム期間中のほぼ１フィールド期間（６ｆ）だけが逆極性で残りの期間（１ｆ～５ｆと７ｆ～８ｆ）は同極性になる。そして、ゲート線Ｙ７上の各画素の印加電圧に対して、その下のゲート線Ｙ８上の各画素に印加されている電圧は図４の第１のフレーム期間について見ると、１フレーム期間中のほぼ２フィールド期間（６ｆ～７ｆ）だけが逆極性で残りの期間（１ｆ～５ｆと８ｆ）は同極性になる。従って、どの走査線に対しても隣接する両側の走査線での逆極性となる期間の合計は３フィールド期間（上側との２フィールド期間と下側との１フィールド期間）とほぼ等しくなる。（但し、各フレーム期間始めの１フィールド期間１ｆにおいて、飛び越し走査で極性が切り替わって選択されるゲート線については、隣接するその直前のゲート線に対して、１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間、或いは１フィールド期間１ｆの開始から書き込みが行われるタイミングまでの期間と１選択期間前の１フィールド期間１ｆの開始から書き込

みが行われるタイミングまでの期間との差の分だけ、逆極性となる期間が僅かに大きくなる。）

このように、各ゲート線上の各画素に印加する電圧は隣り合う上下の各画素に印加する電圧と１フレーム期間中のほぼ１フィールド期間あるいは２フィールド期間だけが逆極性で残りの期間は同極性とする事ができるために、ディスクリネーションラインの発生を低減する事ができ、コントラストの向上、輝度の向上が可能になり、画質を大幅に向上する事ができる。また、チラツキを低減できる。

【００８５】尚、上記実施例は図５（ａ）に示すように各画素に電圧を印加する方法で説明したが、図５（ｂ）に示すようにソース線ごとに極性を反転したり、図５（ｃ）に示すようにソース線２本ごとに極性を反転しても同様の方法で駆動する事ができる。（図５は実施例３に示すように、１フレーム期間を４フィールドに分けて駆動する場合を示しているためにゲート線方向に４画素づつ極性が反転しているが、実施例４ではこれが８画素づつの極性反転に変わる。）（実施例５）上記実施例１から４に示す駆動方法で、１フレーム期間に分割するフィールド数を変えながら表示品質の評価をしたところ、３２フィールドくらいまで分割していくと、ほぼディスクリネーションの影響が無くなり、輝度やコントラストの低下が解消されることが確認できた。

【００８６】また、液晶表示装置の制御回路は、分割するフィールド数が増えるほど複雑になってしまう。

【００８７】これらの事から、分割するフィールド数は２～３２の範囲にすることで、輝度やコントラスト等の表示品質の向上を実現しながら、制御回路の最適化も実現する事ができた。

【００８８】（実施例６）上記、実施例１～５に示した駆動方法による反射型の液晶ライトバルブを使った液晶プロジェクタを作製してして画質の評価をしたところ、輝度とコントラストが向上して画質が大幅に上がった。

【００８９】また、アモルファスシリコンＴＦＴを使った直視型の液晶表示装置を作製して画質の評価をしたところ、輝度とコントラストが向上して画質が上がった。この表示装置をパーソナルコンピュータやテレビに組み込む事によって、画質が向上して見易い電子機器を提供する事ができる。

【００９０】尚、実施例１、２、３、４、６は、１フレーム期間を４フィールドと、８フィールドに分けた場合を例として説明したが、分割するフィールド数は２以上で走査線数以下の整数であればよい。また、走査線数がフィールド数の整数倍にならない場合でも、仮想の走査線を含めて整数倍にしても良いし、各フィールドごとに選択する最後の走査線を選択し終わったら、次のフィールドに行くようにしても良い。

【００９１】また、実施例１～６で示した液晶モード以外の物、例えば、ＴＮモードや４５度ツイストＴＮモードとうに於いても同様の駆動方法で、ディスクリネーションラインを低減して画質を向上する事ができる。

【００９２】また、実施例１～６では、シリコン基板に液晶ドライバを組み込んで、各画素にＭＯＳトランジスタによるスイッチング素子を付けた反射型の液晶ライトバルブを例にして説明したが、アモルファスシリコンＴＦＴやポリシリコンＴＦＴ等のスイッチング素子によるアクティブマトリクスの液晶表示装置であれば同様の駆動方法でディスクリネーションラインを低減して画質を向上する事ができる。また、非線形の２端子素子を使ったアクティブマトリクスの液晶表示装置についても同様の考え方で駆動できる。

【００９３】

【発明の効果】以上述べたように、本発明の液晶表示装置によれば、各ゲート線上の各画素に印加する電圧が隣り合う上下の各画素に印加する電圧と逆極性の期間が電圧を印加している期間全体の中の一部だけで、残りの期間は同極性とする事ができ、逆極性の電圧が印加される期間の長さがどのラインについてもほぼ同じにできるために、ディスクリネーションラインの発生を低減する事ができ、コントラストの向上、輝度の向上が可能になり、チラツキも低減して、画質を大幅に向上する事ができる。

【００９４】また、本発明の電子機器は、輝度やコントラストが向上し、チラツキが低減され、液晶表示装置の画質が大幅に向上して見やすくする事ができる。

【図面の簡単な説明】

【図１】本発明の一実施例で各画素に印加する電圧の極性と電圧書き込みのタイミングを示す図。

【図２】本発明の一実施例で各画素に印加する電圧の極性と電圧書き込みのタイミングを示す図。

【図３】本発明の一実施例で各画素に印加する電圧の極性と電圧書き込みのタイミングを示す図。

【図４】本発明の一実施例で各画素に印加する電圧の極性と電圧書き込みのタイミングを示す図。

【図５】本発明の一実施例で第１のフレーム期間に各画素に印加する電圧の極性を示す図。

【図６】アクティブマトリクス型液晶表示装置の駆動回路と画素の構成の一例を示すブロック図。

【図７】反射型液晶ライトバルブの構成の一例を示す断面図。

【図８】ディスクリネーションラインの発生の様子を示す図。

【図９】従来駆動での各画素に印加する電圧の極性を示す図。

【符号の説明】

６０１．画素部の等価回路

６０２．トランジスタ

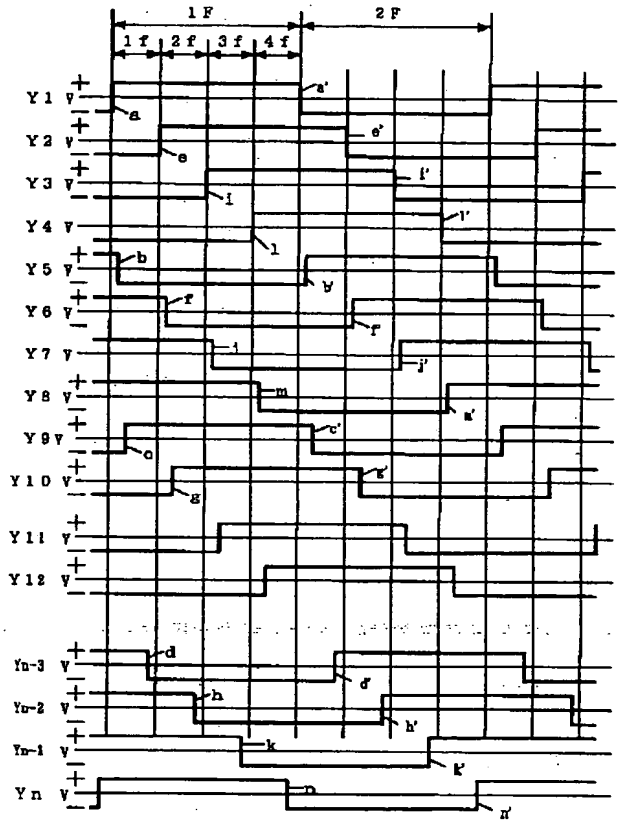
６０３．ゲート

６０４．ソース

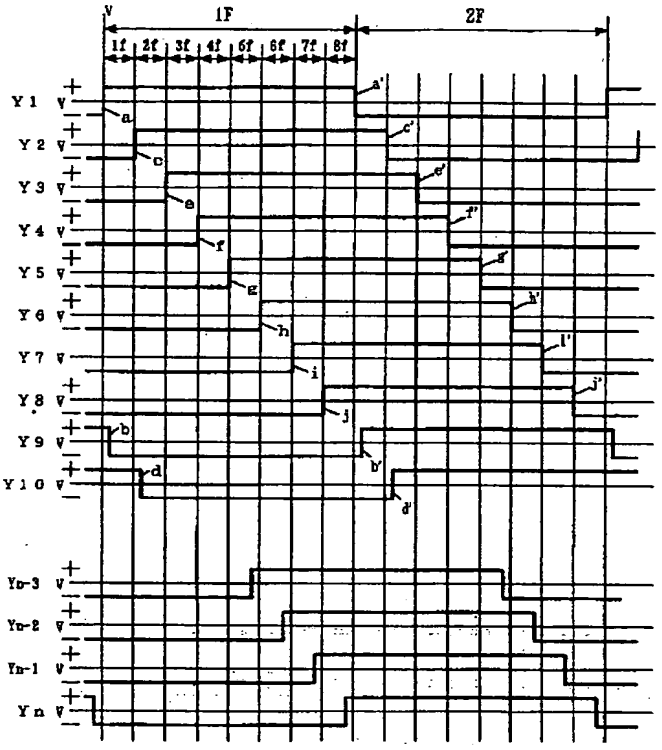
６０５．ドレイン及び画素電極
６０６．液晶
６０７．保持容量
６０８．共通電極
６１１．信号線ドライバ
６１２．ゲート線ドライバ
６１３．画素部
６１４．ゲート線

６１５．ソース線
７１．　偏光手段
７２．　ガラス基板
７３．　透明電極
７４．７６．配向膜
７５．　液晶
７７．　シリコン基板

【図１】

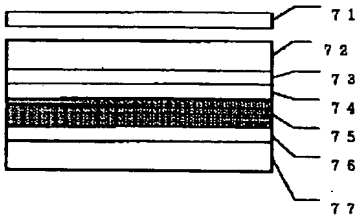


【図２】

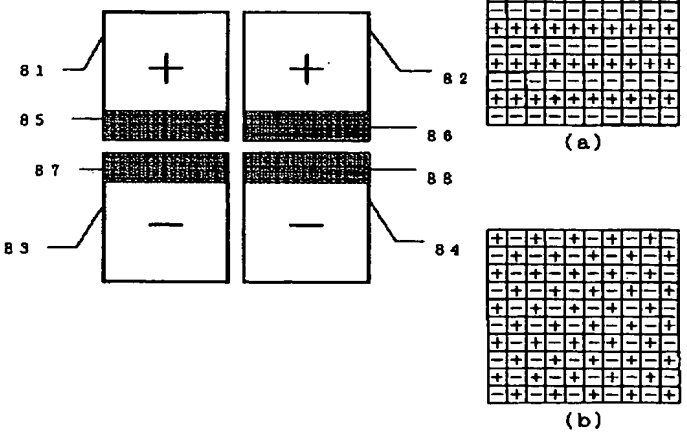


【図９】

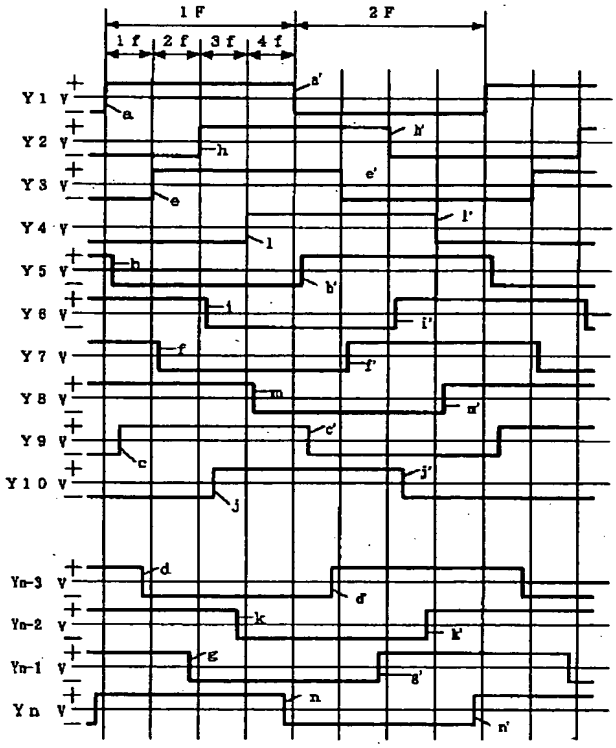
【図７】



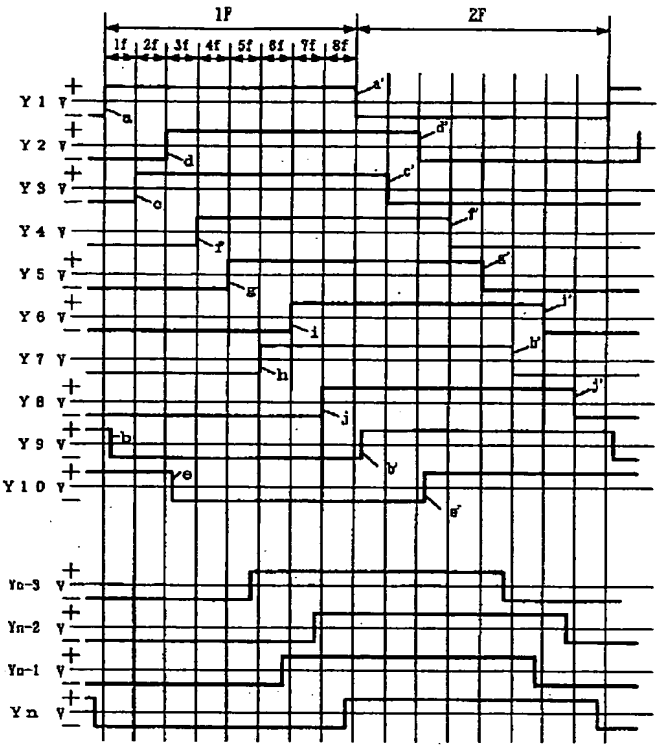
【図８】



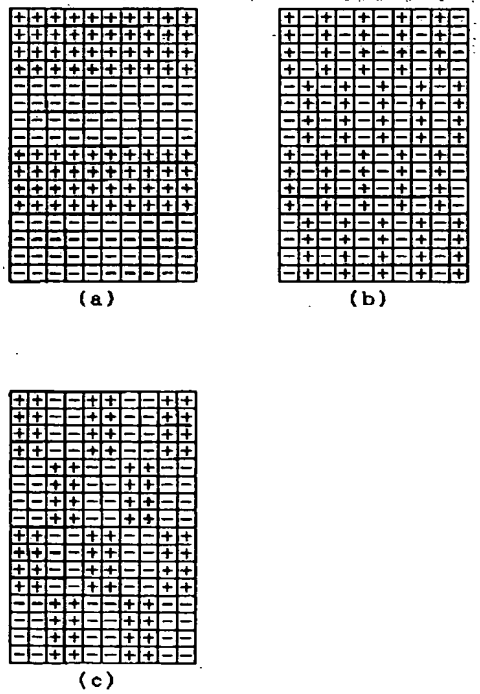
【図３】


1 F
2 F
1 f
2 f
3 f
4 f
Y 1 V
Y 2 V
Y 3 V
Y 4 V
Y 5 V
Y 6 V
Y 7 V
Y 8 V
Y 9 V
Y 10 V
Yn-3 V
Yn-2 V
Yn-1 V
Yn V

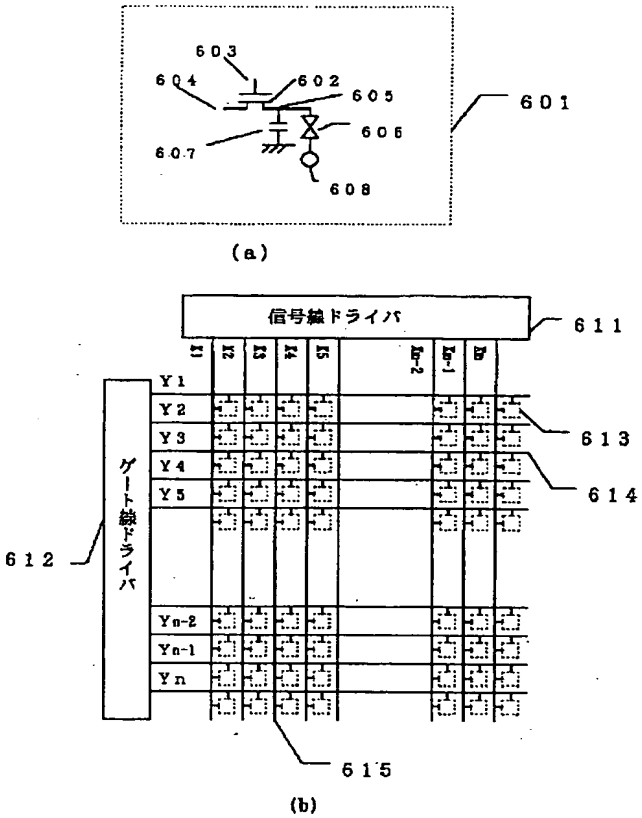
【図４】


1F
2F
1f
2f
3f
4f
5f
6f
7f
8f
Y 1 V
Y 2 V
Y 3 V
Y 4 V
Y 5 V
Y 6 V
Y 7 V
Y 8 V
Y 9 V
Y 10 V
Yn-3 V
Yn-2 V
Yn-1 V
Yn V

【図５】


(a)
(b)
(c)

【図６】


603
604
602
605
606
607
608
601
(a)
信号線ドライバ
611
X1
X2
X3
X4
X5
Xm-2
Xm-1
Xm
Y1
Y2
Y3
Y4
Y5
Yn-2
Yn-1
Yn
ゲート線ドライバ
612
613
614
615
(b)